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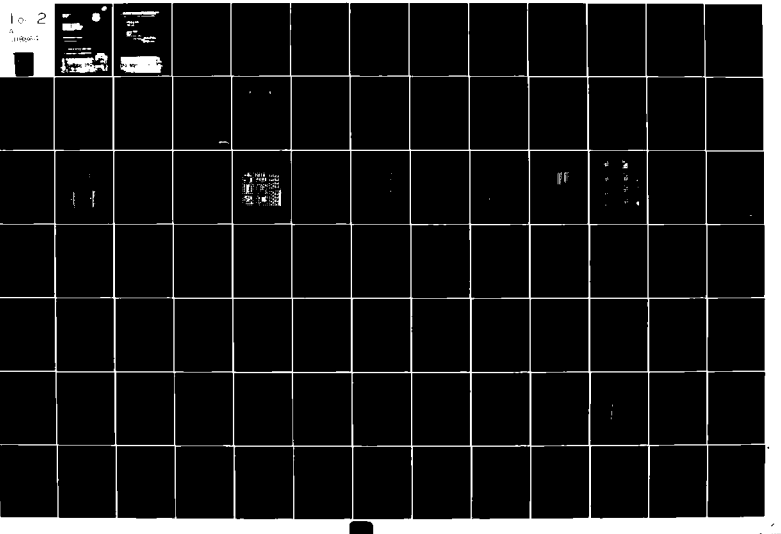

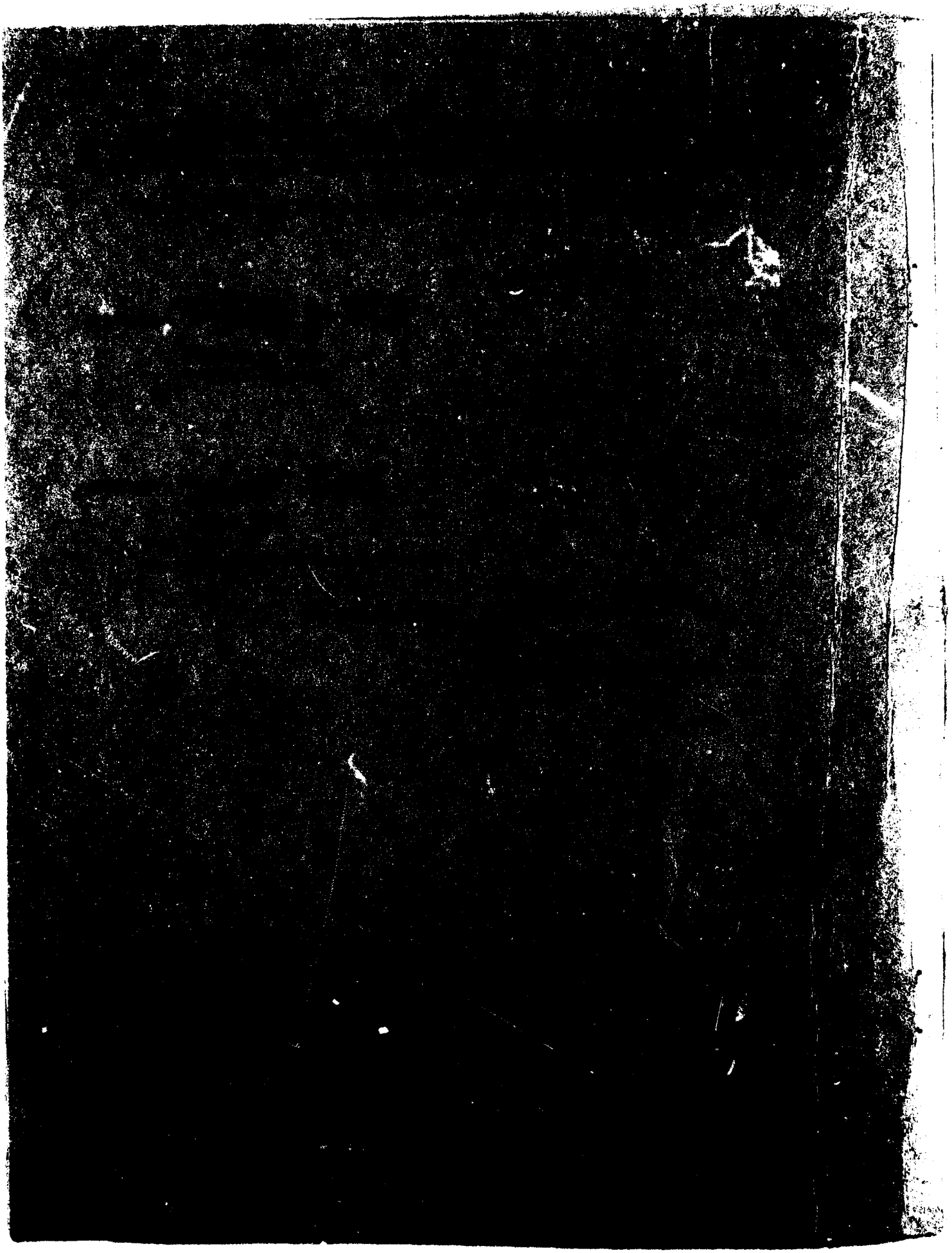

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

In this investigation the endurance-retention characteristics of fast-write MNOS memory structures, radiation tolerance of metal-gate dual-dielectric and polysilicon-gate all-oxide devices have been evaluated. Writing and clearing speed have been studied with respect to the NH_3:SiH_4 ratio (APCVD), and NH_3:$SiCl_2H_2$ ratio (LPCVD). The films deposited with a low NH_3:$SiCl_2$ ratios could be written and cleared with shorter pulse widths; however a degradation in retention was observed.

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An improvement in the endurance retention product of a drain source protected transistor structure has been realized by oxidizing the memory nitride followed by an H_2 anneal immediately after deposition. The film was deposited with a LPCVD reactor at 750°, with a NH_3:$SiCl_2H_2$ ratio of 9:1. Oxidation was performed in steam at 900°C, as was the subsequent H_2 anneal.

The effect of total dose radiation was found to be more severe for a positive bias. The all oxide polysilicon gate transistor structures were observed to be relatively "soft", however results from capacitor structures shows promise in developing a radiation tolerant polysilicon-gate all-oxide gate structure.

Item 19 (Cont'd)

Atmospheric Pressure Chemical Vapor Deposition (APCVD)
Drain Source Protected (D&P)

750 deg

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I. INTRODUCTION

The "MNOS/SOS Radiation Hardness Reliability Study" research and development program is directed toward improving the radiation hardness, performance and reliability of nonvolatile semiconductor memory.

In developing a device technology that is to be used to produce devices that will provide a required performance, there is a need for a sufficient amount of reliable performance data. From a reliable data base, device performance can be predicted and insight into the physics of operation is also obtained. This development approach involves establishing a data base which will be used to develop and verify physical models. The data and models will allow circuit designers to develop improved radiation hardened MNOS/SOS memories to satisfy a wide range of performance requirements for satellite, missile, and re-entry applications. The performance objectives for the MNOS/SOS technology are a total dose hardness to 10^6rad (Si), dose rate survival of data to 10^{12} rads (Si)/sec, write cycle time in lusec, read access time of 250 nano-seconds and retention of 24 hours after 10^{12} write reversals.

During the period of the program covered by this report, effort was focused on both memory and non-memory capacitor and

transistor device types. Devices have been fabricated in both bulk silicon substrate and silicon on sapphire (SOS), using a metal gate process. The polysilicon gate results to be reported are all fabricated in bulk silicon substrates. Most of the polysilicon gate data was derived from capacitors, fabricated in bulk silicon. The process variables that were considered included two nitride types, (Low Pressure Chemical Vapor Deposited films - LPCVD and Atmospheric Pressure Chemical Vapor Deposited films - APCVD) deposited with various gas ratios, and various anneal atmospheres and temperatures. Non-memory devices consisted of either an all oxide structure or a dual layer structure consisting of an oxide film over which a nitride is deposited. The thickness of the two films depends on the process being used.

As mentioned earlier, the bulk of the data is from capacitor structures which were fabricated in bulk silicon substrates. 90% of the Memory Transistor data, however, were obtained from devices fabricated in SOS substrates. Measurements that were made consist of the memory pulse response, memory retention, the charge distribution in the nitride films, temperature - bias stress stability, accelerated d. c. endurance stress characteristics and pulsed endurance stress characteristics. Total dose radiation testing has been performed on dual dielectric oxide/nitride metal gate transistor structure, all oxide polysilicon gate capacitor structures and all oxide polysilicon gate transistors processed

with an existing polysilicon gate CMNOS process and test pattern.

The density of traps in a Si_3N_4 film can be varied by changing the ammonia (NH_3) to silane (SiH_4) ratio in an APCVD film and the ammonia (NH_3) to dicholrosilane ($SiCl_2H_2$) ratio for the LPCVD structures. The speed in which the devices can be written can be increased. However, a degradation in charge retention is experienced. The clear/write endurance cycles of metal gate MNOS memory transistors was improved by annealing the memory nitride in a 100% H_2 ambient at 900^oC. The structures annealed in H_2 have been stressed to 10^{11} cycles with minimum amount of degradation in the memory characteristics. The negative threshold voltage of a dual dielectric metal gate transistor structure was found to be less than -2V for a total dose radiation level of about 100K rads of silicon with a negative gate voltage $-V_{GS}$. The effect of the positive bias was much more severe than the negative bias. The n-channel polysilicon gate transistor structures shifted into depletion mode at relatively low total dose radiation level. The low radiation tolerance is believed to be due to a high temperature reflow step performed after the gate oxide has been grown.

2. THEORY

Numerous theoretical models have been advanced to describe the write erase operations of a MNOS memory device. A common agreement, however, is reached by each of the investigators proposing the different models, i.e. electrons and holes (under positive and negative bias respectively) are transported via a tunneling mechanism through the silicon dioxide into the silicon nitride. Here, the charge can become trapped by the silicon nitride, which results in a stored charge in the dielectric. This stored charge in turn produces a shift in the flatband voltage or threshold voltage in MNOS capacitors and/or transistors.

The schematic in Figure 2-1 illustrates the MNOS device structure and its electronic energy band diagram. When a positive bias is applied to the gate, electrons are injected across the oxide barrier and can become trapped in the nitride layer. The trapped electrons are manifested by a positive shift in the flatband voltage relative to its present position. The effect to a negative bias on the gate is the opposite. Holes are transported and trapped, resulting in a negative shift in the flatband voltage. The shift in flatband voltage can be written in terms of the trapped charge in the nitride, Q_n, and the average distance the charge is trapped into the nitride, $\bar{d}$. The equation depicting the relationship is,

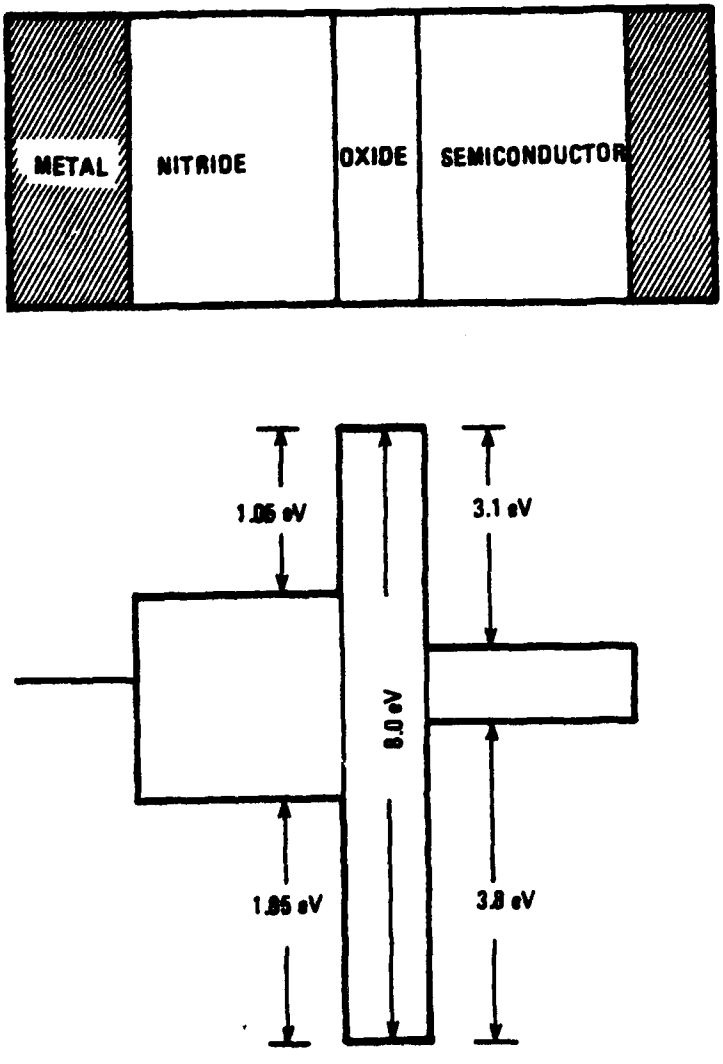


Figure 2-1. Electronic energy band diagram of MNOS Structure

$$V_{FB} = -Q_N(X_N - \bar{d}) / \epsilon_N \qquad 2\text{-}1$$

Here ϵ_N is the nitride permitivity and X_n the thickness of the nitride film.

The electric field that is impressed across the nitride is impacted by the change in the flatband voltage coupled with the space charge region of the trapped charge. Because the region in the nitride over which the voltage is dropped becomes effectively smaller as the centroid of charge moves deeper into the film, the nitride field tends to increase. The relationship describing the field in the nitride taking into account the trapped charge, or the maximum field in the nitride, E_{NM} is,

$$E_{NM} = (V_g + V_{FB}\, \bar{d} / \bar{X}_N)/\bar{X}_N \qquad 2\text{-}2$$

where V_g is the applied gate voltage during charge injection, $\bar{X}_N = X_N - \bar{d}$, and the remaining terms having been defined earlier.

With the empirical derived linear relationships of Q_N and $\bar{d}$ as a function of E_{NM}, and equation 2-1, the change in flatband voltage can now be expressed as a function of E_{NM}, giving;

$$V_{FB} = A_2 E_{NM}^2 + A_1 E_{NM} + A_0 \qquad 2\text{-}3$$

Where:

$$A_2 = K_g K_d / \epsilon_N$$

$$A_1 = K_q (X_d - X_N - E_{TH} K_d) / \epsilon_N$$

and

$$A_0 = K_q E_{TH} (X_N - X_d) / \epsilon_N$$

The constraints K_q, K_d, X_d and E_{TH} are independent of nitride field and thickness and can be determined experimentally. [1,2,3]

The charge retention or charge decay may be expressed in terms of the nitride, J_n and oxide, J_o current density, [4] i.e.

$$\sigma_t = -\partial Q_n / \partial t = J_n + J_o \qquad 2\text{-}4$$

The equation describing the decay rate by combining the various conduction mechanisms associated with the oxide and nitride is given by:

$$\sigma_t / X_n = \partial n_t(x,t)/\partial t = J\,\lambda/E(N_t - n_t(x,t)) - n_t(x,t)\,\nu$$

$$\cdot \mathrm{Exp}(-q/kT(\phi - \beta\sqrt{E})) - n_t(x,t)e^{-\alpha x} / \tau_1 \qquad 2\text{-}5$$

where λ, ν, β, α and τ_1, are constants related the material, n_t is the density of trapped charge, ϕ the trap energy depth and q is the unit electronic charge. Two additional equations are required to obtained a solution to equation 2-5. They are Poisson's equation.

$$-\partial^2 V / \partial x^2 = \partial E / \partial x = \rho / \varepsilon \qquad 2\text{-}6$$

and the continuity equation modified to the form,[5]

$$-\partial J / \partial t = \partial n_t / \partial t + n_t \cdot e^{-\alpha x} / t_1 \qquad 2\text{-}7$$

It has been demonstrated, however, that at room temperature decay rate can be approximated by the following [6]

$$\sigma_t = \sigma_i \left(1 - \ln(t/t_d) / \alpha_N X_N \right) \qquad 2\text{-}8$$

The constants α_N, t_d and σ_i are related to the material. A detailed discussion of these constants is found in reference 6.

3. EXPERIMENTAL APPROACH

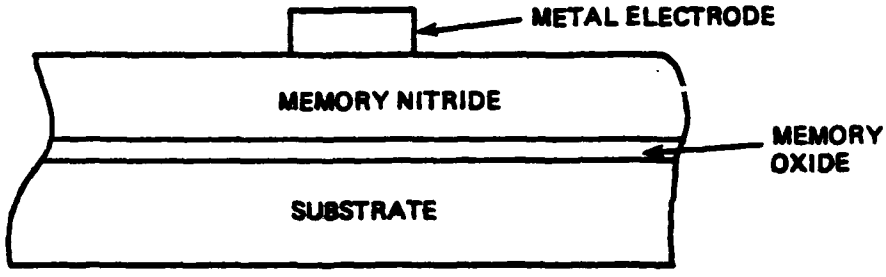
A matrix of process variables has been established for various types of memory gate and non-memory gate insulator structures. Included are various nitride formation conditions using APCVD and LPCVD techniques, post dielectric deposition thermal anneals, and oxide-nitride interface barrier modification and formation. In addition to single nitride formation, two step nitride deposition schemes have also been investigated.

3.1 Device Cross Sections and Process Variables

The following discussions and illustrations will describe the different structures and variations in process parameters that have been investigated.

The structure used to determine the density of trapped charge, charge centroids, trapping length and trap cross sections is shown in Figure 3-1. These parameters were determined for both APCVD nitrides and LPCVD nitrides where the process variables were different NH_3 to SiH_4 and NH_3 $S_iCl_2H_2$ ratios respectively.

The APCVD films were deposited with NH_3:SiH_4 ratios of 28:1, 150:1, 300:1, and 450:1. NH_3: $SiCl_2H_2$



LOT 4071
LOT 4112
LOT 4193

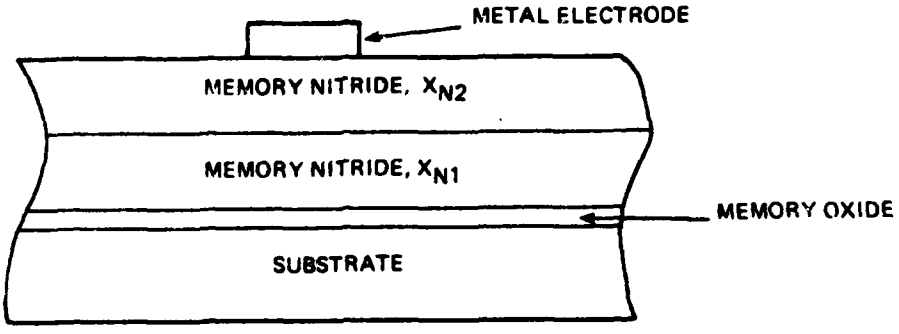
LOT NO.	NH_3: RATIO	NITRIDE THICKNESS (ANGSTROMS)
4071	NH_3: $SiCl_2H_2$ = 9:1	401, 605, 824, 1006
4193	NH_3: $SiCl_2H_2$ = 3:1	337, 541, 716, 933
4112	NH_3: SiH_4 = 28:1	400, 634, 852, 994
	NH_3: SiH_4 = 150:1	461, 671, 881, 1023
	NH_3: SiH_4 = 300:1	432, 625, 859, 1102
	NH_3: SiH_4 = 450:1	380, 580, 790, 1025

80-0945-VA-2

Figure 3-1. Capacitor gate structures and process variables used to determine N_{tst} (0), d, x_o and V_t

ratios of 3:1 and 9:1 were used for the LPCVD nitrides. The diagram in Figure 3-2 shows the cross section for the structures containing the two step nitrides. The one case consisted of two layers with one (X_{n1}) more conductive than the other (X_{n2}). One structure contained as a first layer an APCVD nitride with a NH_3:SiN_4 ratio of 28:1 and a second layer of LPCVD nitride with a NH_3:$SiCl_2H_2$ of 9:1. The two step all LPCVD structure included a first layer with a NH_3:$SiCl_2H_2$ ratio of 3:1 and a second layer with a NH_3:$SiCl_2H_2$ = 9:1. The two step structure was also used to investigate the extent annealing thin layers, (25A to 50A), of silicon nitride influenced the electronic barrier at the oxide - nitride interface. The process parameters consisted of various gases and temperatures, in which either the first layer only or both layers were subjected to the anneal step.

The polysilicon gate process required the structures depicted in Figure 3-3 and 3-4. In Figure 3-3 the polysilicon before memory nitride process cross section is shown. The non-memory gate insulator is an all oxide structure. The process variables consisted of polysilicon thickness, phosphorous doping source and doping times. The cross sections in Figure 3-4 gives those structures that were used with polysilicon after memory nitride process. The non-memory gate insulator structure consists of an oxide over which the memory nitride is deposited. Note that in the polysilicon after memory nitride process, the memory nitride will undergo two



LOT 4236
LOT 4193
LOT 01

- LOT 4236
  X_{N1} = 103 A APCVD (NH_3: SiH_4 = 28:1), X_{N2} = 410 Å LPCVD (NH_3: $Si Cl_2H_2$ = 9:1)
  X_{N1} = 172 A APCVD (NH_3; SiH_4 = 28:1), X_{N2} = 299 Å LPCVD (NH_3:$SiCl_2H_2$ = 9:1)
- LOT 4193
  X_{N1} = 200 A LPCVD (NH_3: $SiCl_2H_2$ = 3:1), X_{N2}=103 Å LPCVD (NH_3 : $SiCl_2H_2$ = 9:1)
  X_{N1} = 200 A LPCVD (NH_3:$SiCl_2H_2$= 3:1), X_{N2} = 204 Å LPCVD (NH_3 : $SiCl_2H_2$ = 9:1)

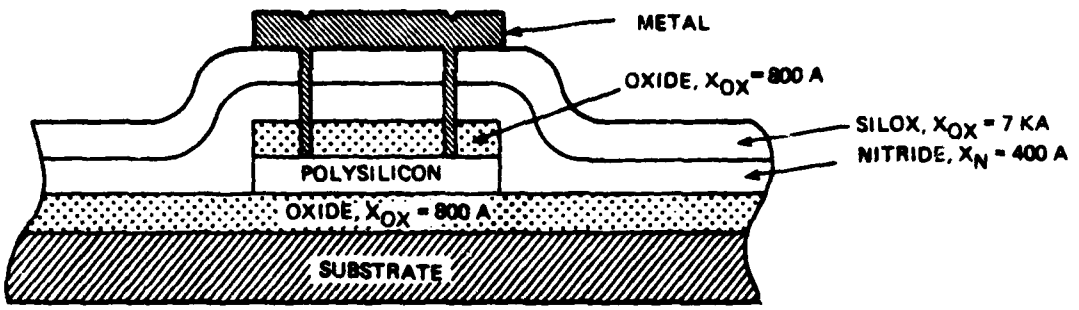
80-0945-VA-3

Figure 3-2. (a) Gate structure and process variables for two step nitrides.

0 LOT 01					
X_{N1}	ANNEAL AMBIENT	TEMP	X_{N2}	ANNEAL AMBIENT	TEMP
29 A	H_2	900°C	391 A	None	None
29	H_2	900	391 A	H_2	900°C
29	N_2	900	391 A	None	None
29	NH_3	900	391 A	None	None
29	NH_3	1100	391 A	None	None
51	H_2	900	391 A	None	None
51	H_2	900	391 A	H_2	900°C
51	N_2	900	391 A	None	None
51	NH_3	900	391 A	None	None
51	NH_3	1100	391 A	None	None

80-0945-VA-4

Figure 3-2. (b) Process variation for two step barrier modification structures.



o LOT 4366 AND 4276

POLYSILICON THICKNESS	DOPING SOURCE	DRIVE TIME	TEMP
3.8K	PHOSPHINE	15 MIN	900°C
3.8K	PHOSPHORUS GLASS	40	900
3.8K	PHOSPHORUS GLASS	25	900
6.1K	PHOSPHINE	15	900
6.1K	PHOSPHORUS GLASS	40	900
6.1K	PHOSPHORUS GLASS	25	900

80-0945-VA-5

Figure 3-3. Gate structures and process variables of polysilicon before memory nitride process.

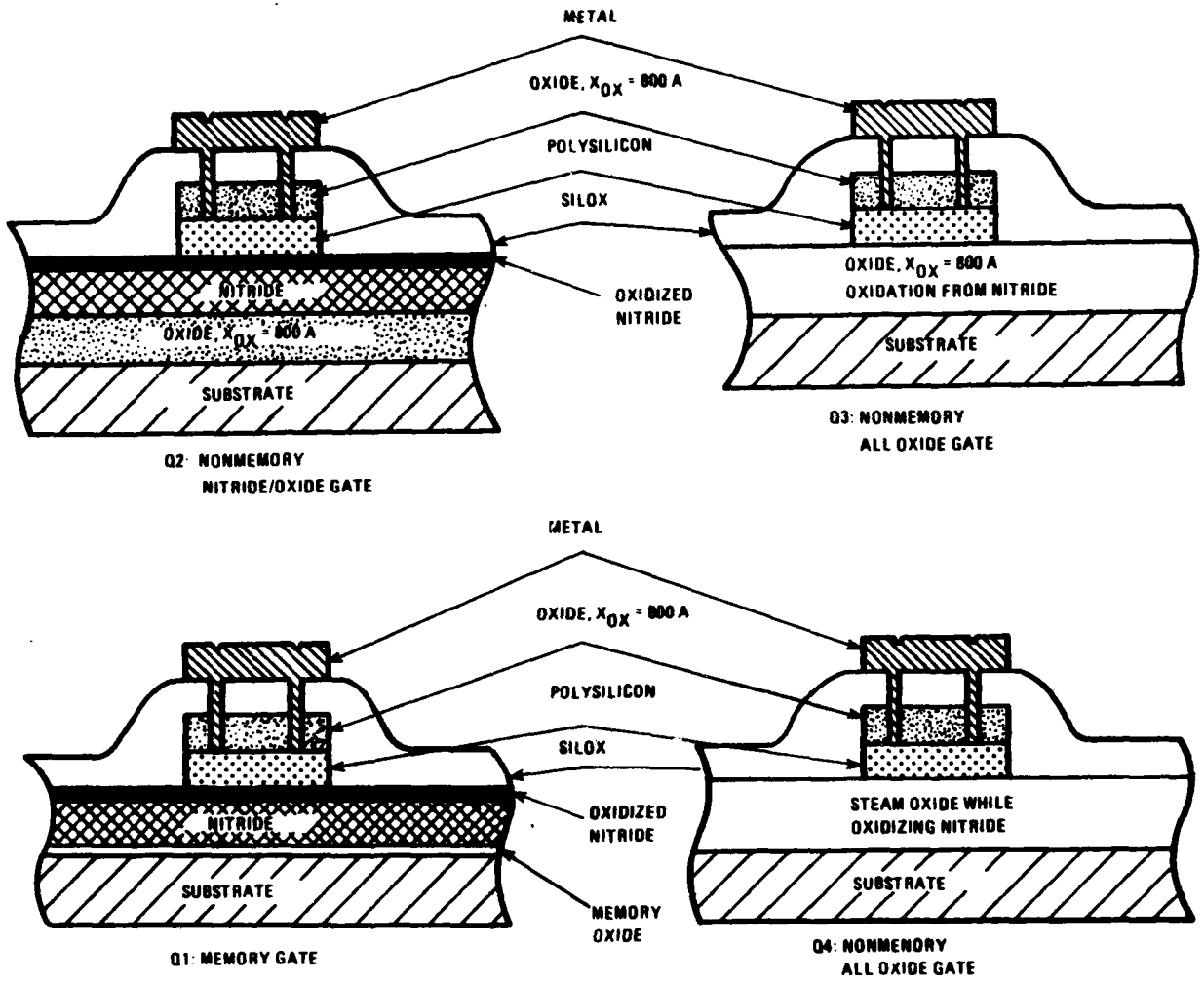


Figure 3-4. Gate structures of polysilicon after memory nitride process. 80-0945-VA-6

additional temperature steps when compared to the polysilicon before memory nitride process. The two additional steps are the polysilicon deposition and doping sequences

The test pattern to be used with the X-ray Photoelectron Spectroscopy (XPS) work is shown in Figure 3-5. With this design capacitors are fabricated that can be stressed electrically with both polarities. Several size capacitors are available which allow various electrical tests and XPS experiments to be performed.

3.2 Test Pattern Descriptions

The 6203T is a MNOS/SOS device test pattern designed to characterize the electrically programmable non-volatile memory. Figure 3-6 presents a global view of the test vehicle. A test pattern containing continuity checks, contact window tests, resistor strings and a N^- substrate thick field capacitor is available. Figure 3-7 shows the test structures found in test pattern 2. Included are P and N-channel enhancement mode transistors, with various channel lengths and widths, P+ and N+ dogbones, P^- and N^- substrate thick field capacitors. Test pattern 3 is shown in Figure 3-8 to contain N-channel depletion and enhancement mode device, P-channel enhancement mode devices, an input protect network and continuity checks of the P+, N+ and metal. N-channel depletion mode and enhancement mode devices, PSM memory subcells, memory

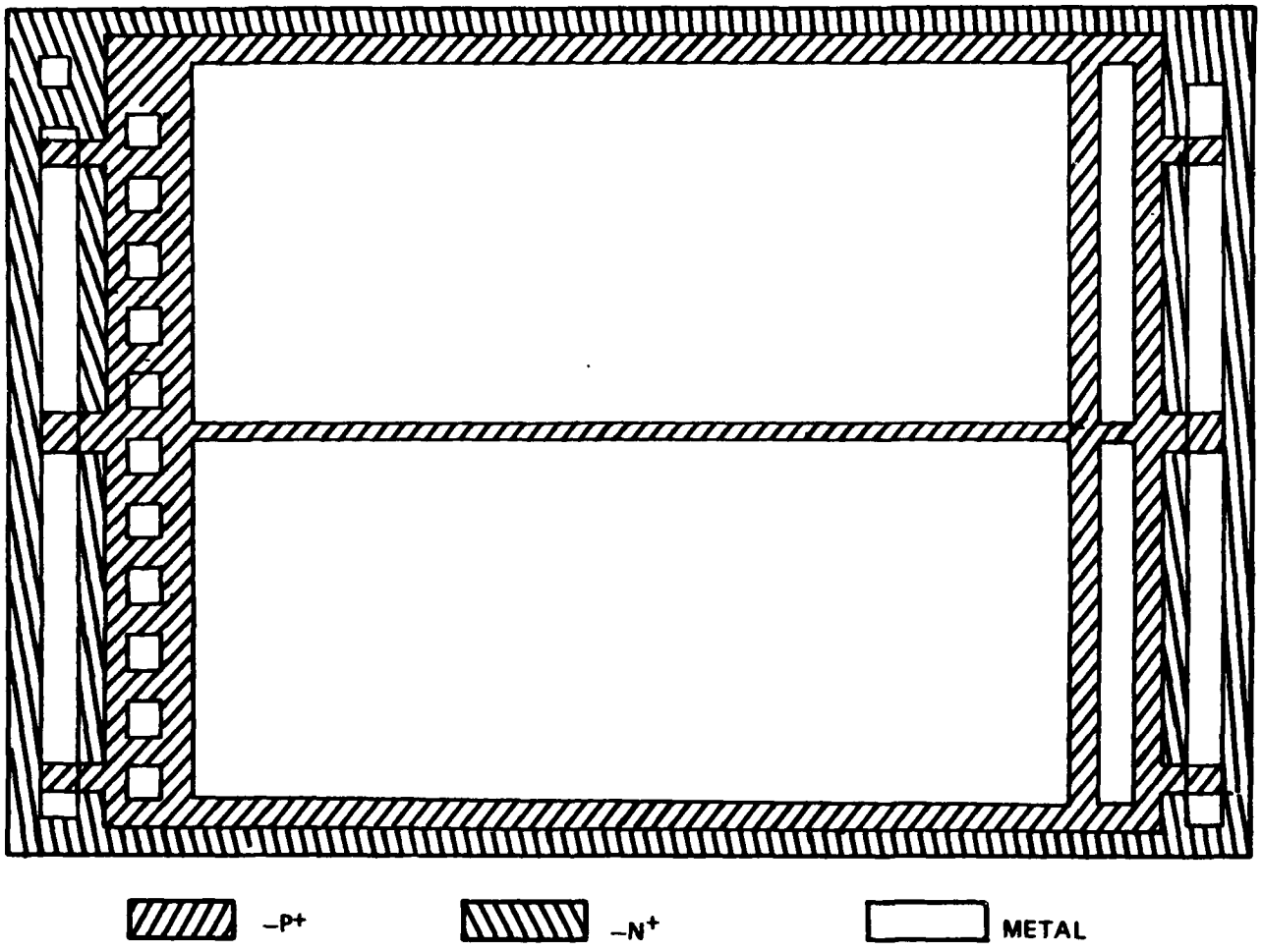


Figure 3-5. X-ray Photoelectron Spectroscopy (XPS) test pattern.

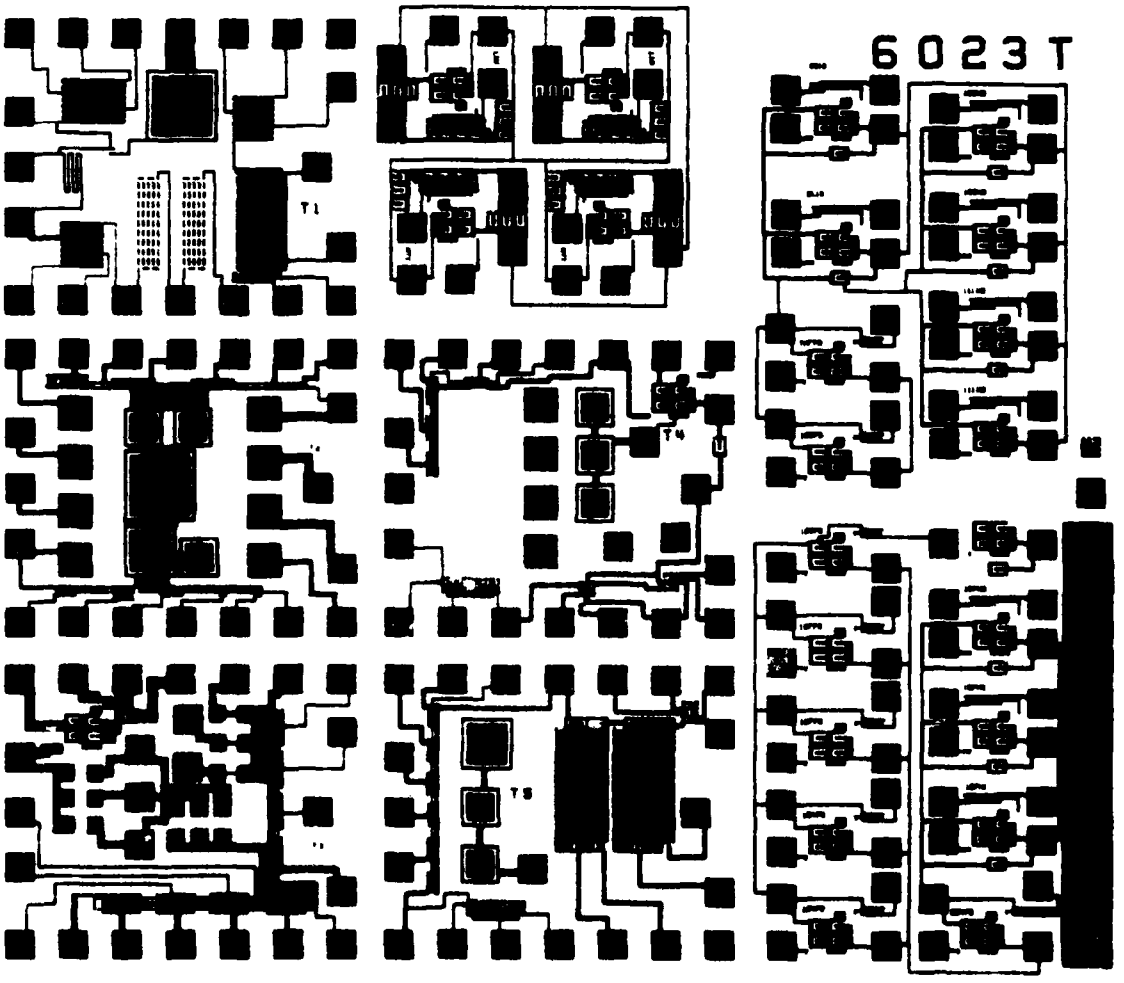


Figure 3-6. 6023T MNOS/SOS memory test vehicle.

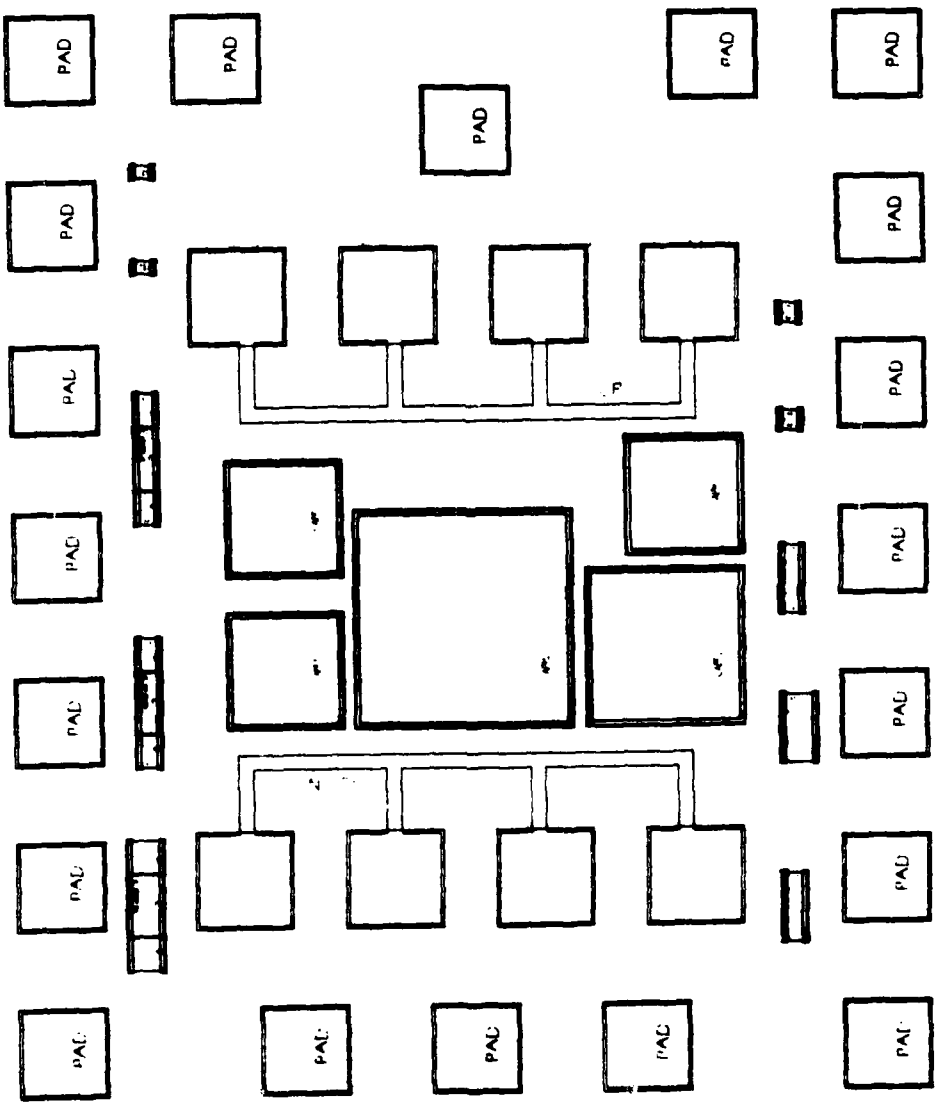


Figure 3-7. In-line process control test pattern 2.

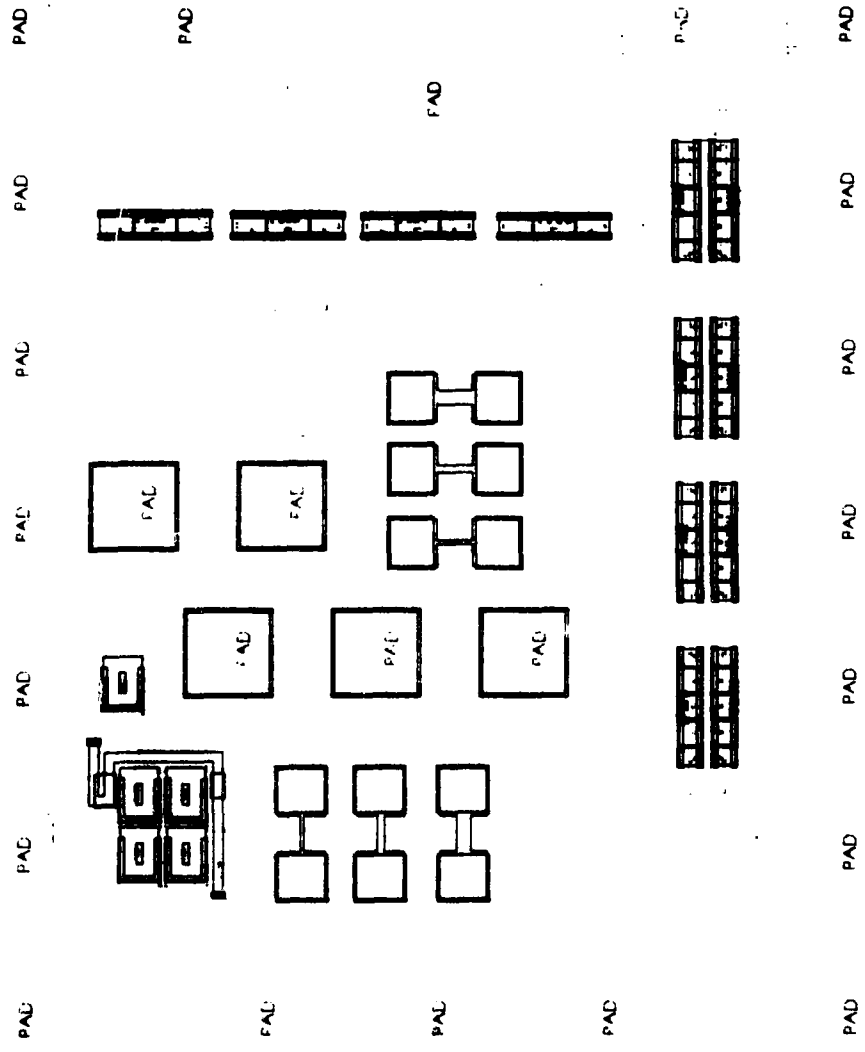


Figure 3-8. In-line process control test pattern 3.

capacitor structures, input protect network and diode, and a P^- dogbone are found in test pattern 4, Figure 3-9. In Figure 3-10, test pattern 5 is shown to have large N-channel and P-channel Drain Source protected memory transistors, PSM memory subcells, various capacitor structures and P-channel enhancement mode devices. Non-memory transistors with input protect circuitry test structures are shown in Figure 3-11, for P-channel enhancement mode and N-channel depletion mode devices. The memory transistor structures are shown in Figure 3-12. These devices are identical to those used in the memory, but containing only four transistors.

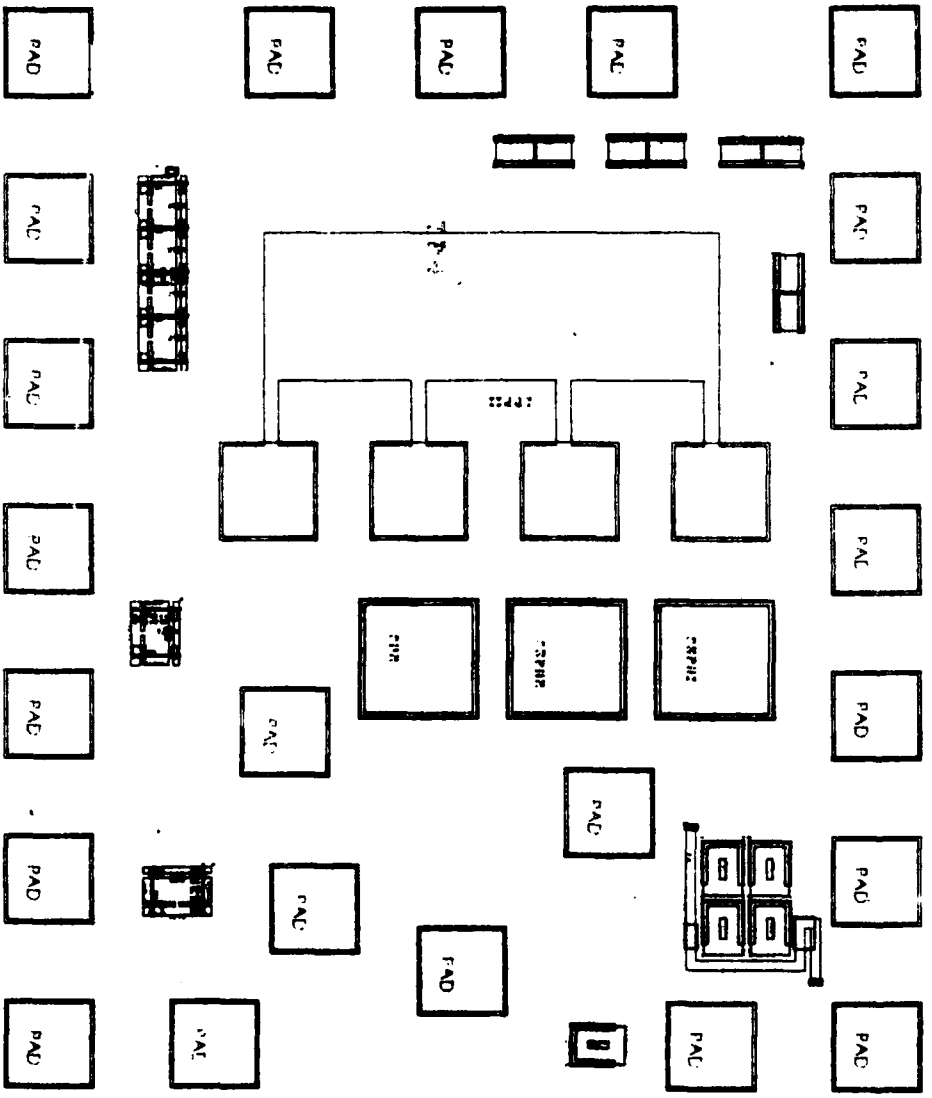


Figure 3-9. In-line process control test pattern 4.

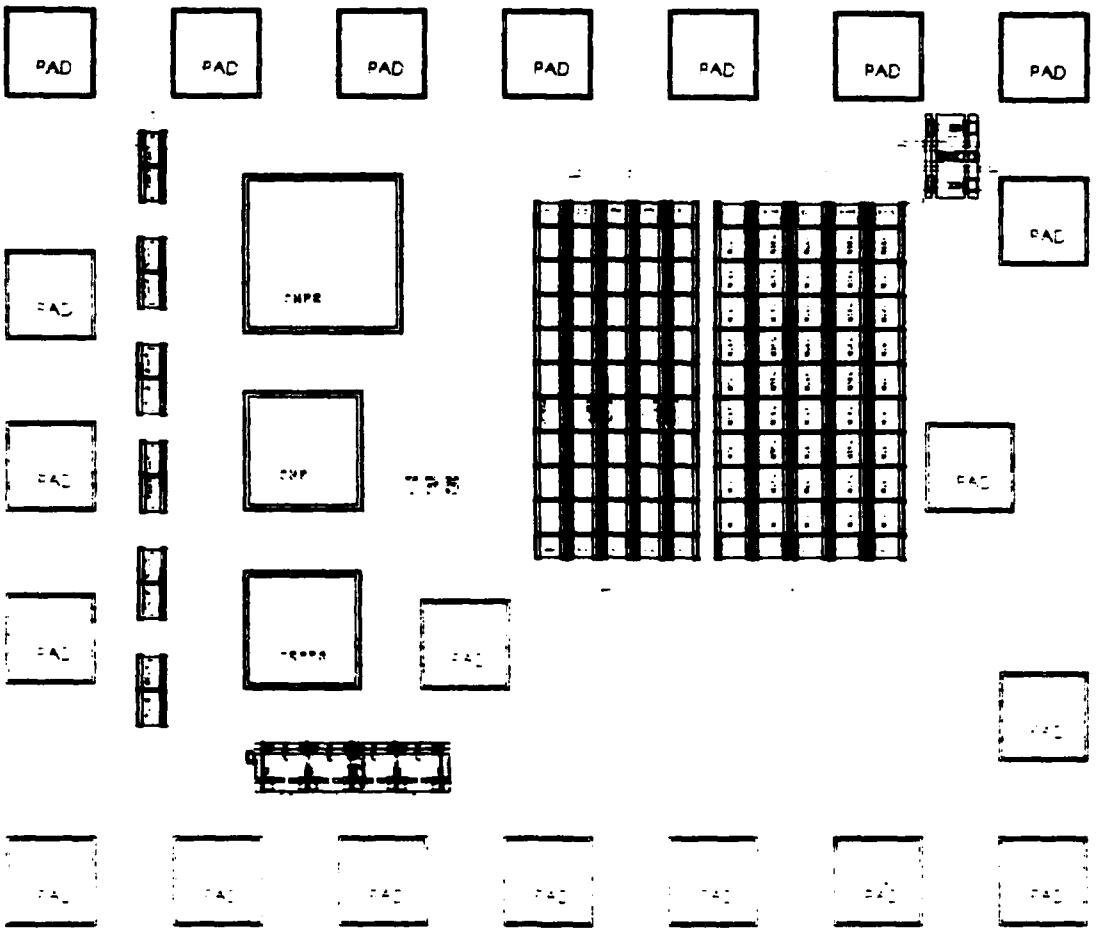


Figure 3-10. 6023T in-line process control test pattern

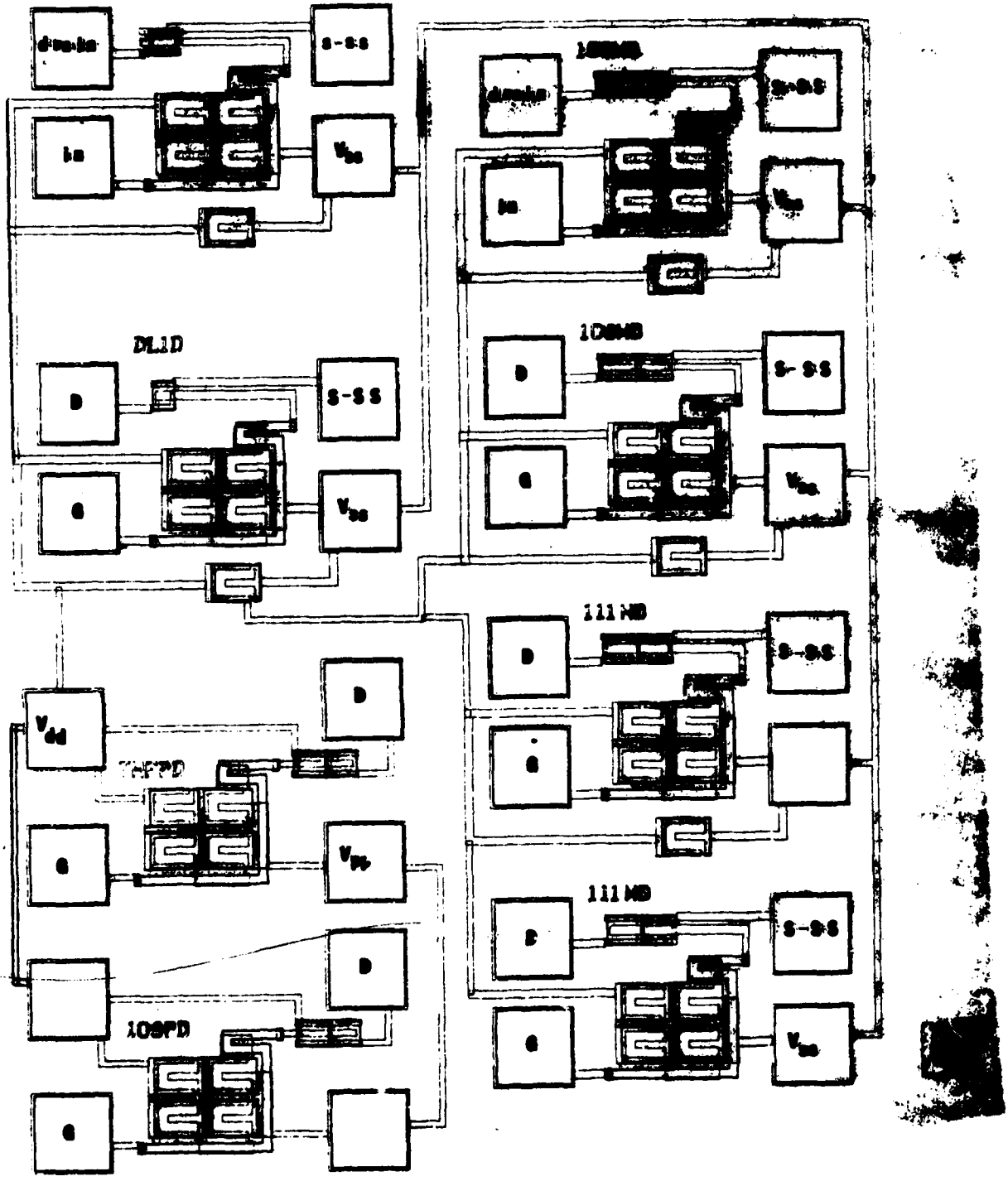


Figure 3-11. Non-memory P-channel enhancement mode and N-channel depletion mode test structures.

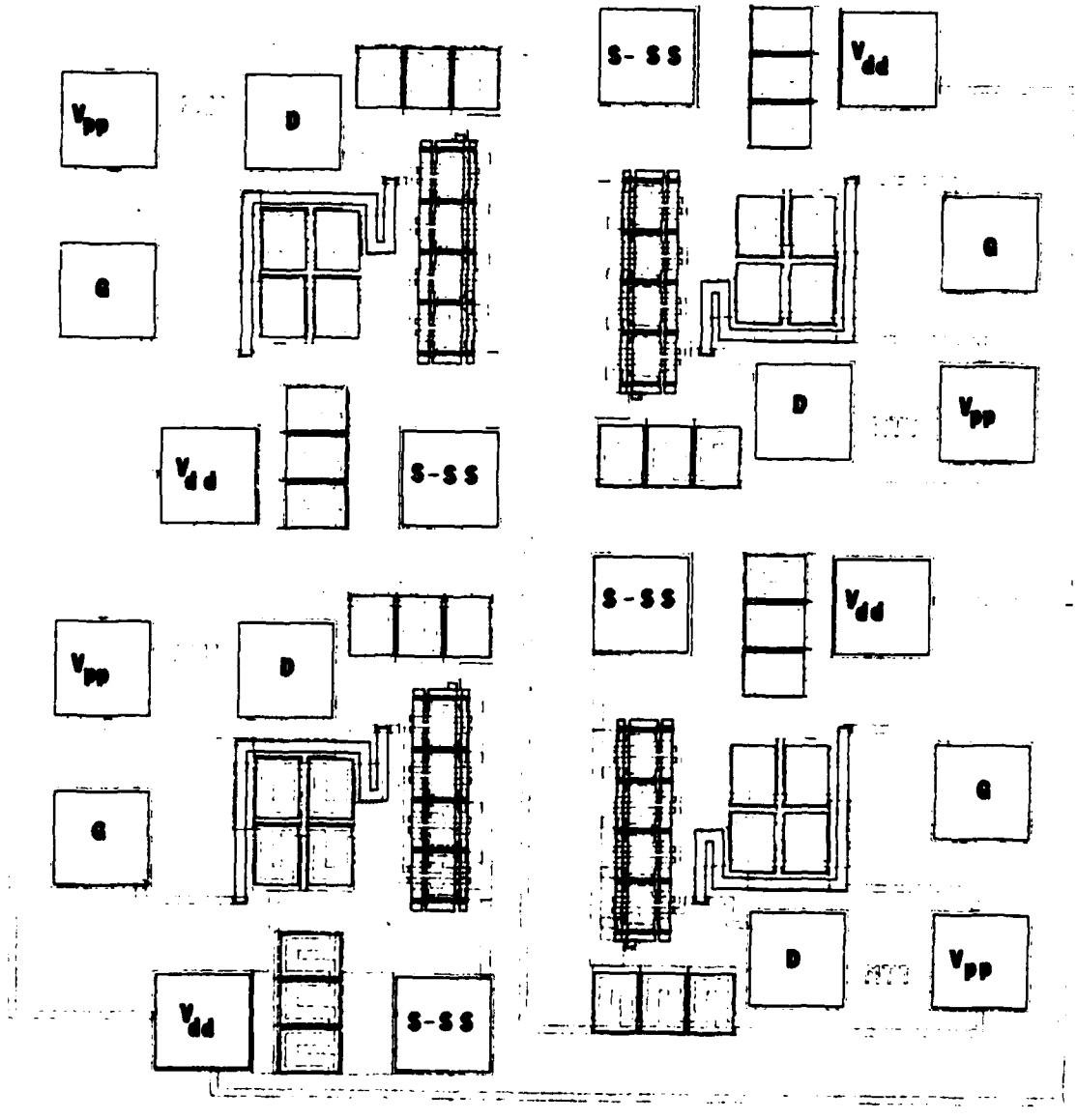


Figure 3-12. In-line process control memory array subcell structure

4.0 EXPERIMENTAL DATA

4.1 Charge Trapping in Nitride

The density of trapped charge and trapping length is plotted as a function of NH_3:SiH_4 ratio for APCVD nitrides in Figure 4-1 and NH_3:$SiCl_2H_2$ ratio for LPCVD nitrides in Figure 4-2. It is noted that the density of trapped charge decreases while the trapping length increases as the NH_3:SiH_4 ratio increaes for the APCVD films. The same trend is observed for NH_3:$SiCl_2H_2$ ratios for the LPCVD nitride. These data are summarized in Table 4-1 where the trap cross sections are also given. In Figure 4-3 the density of trapped charge is plotted as a function of the charge centroid at various temperatures for a 9:1 (NH_3:$SiCl_2H_2$) LPCVD film. It is observed that the electron charge centroid is influenced by temperature to a larger degree than holes. At room temperature the hole centroid is larger than electrons, however, at 125°C the electron centroid has become larger, and the density of trapped charge has decreased. The minimum nitride thickness is shown as a function of the slope of the charge density vs centroid curves $\partial Q_n / \partial \bar{d} = S$, and X_o in Figure 4-4 at 25°C. An arbitrary stored charge level to $1uC/cm^2$ was chosen because of the lack of detrapping in the nitride even at relatively high fields. The minimum nitride thickness is shown to approach twice the trapping length

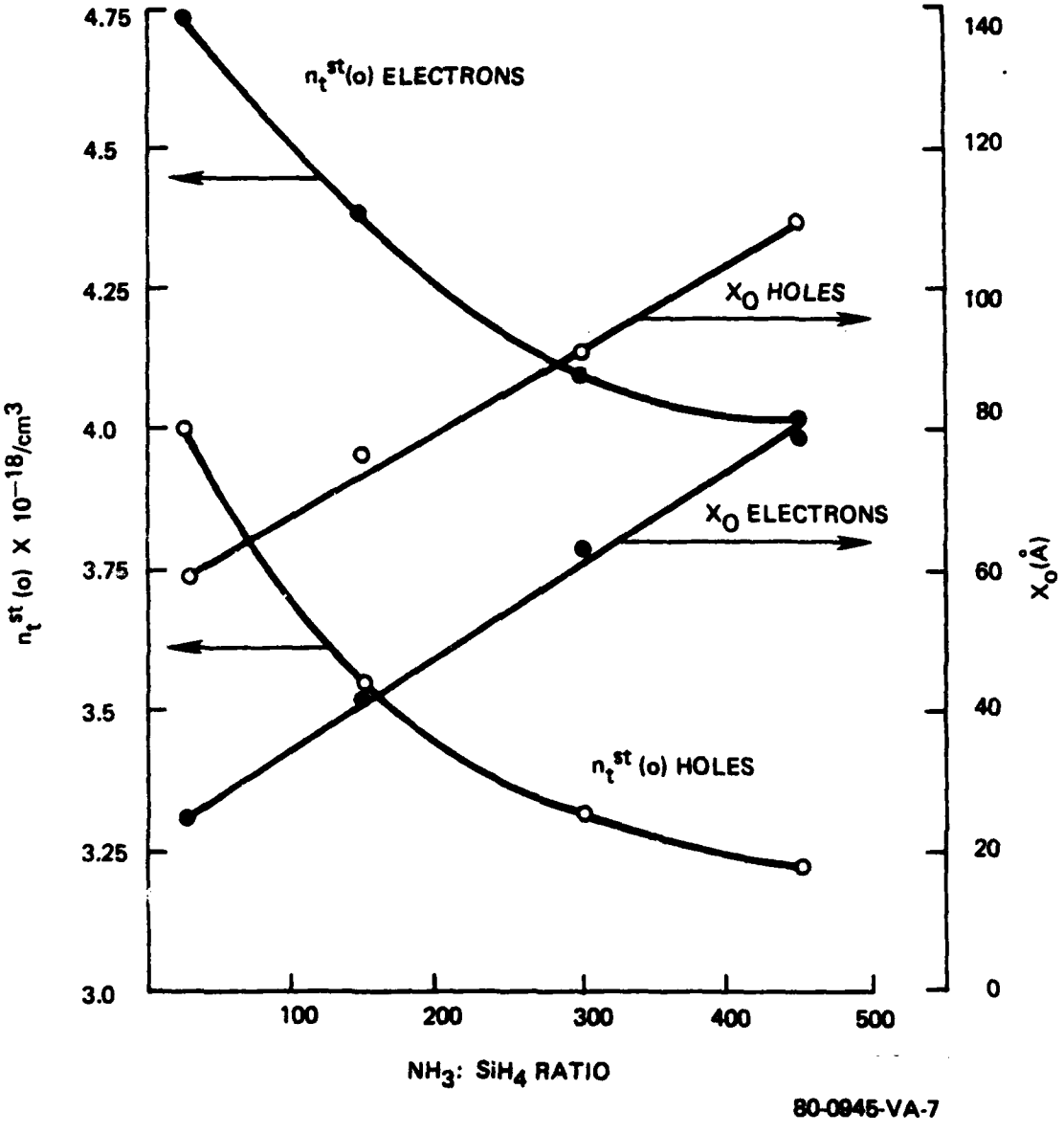


Figure 4-1. $N_{t}s^{t}$ (O) and X_o vs. NH3:SiH_4 ratio (APCVD)

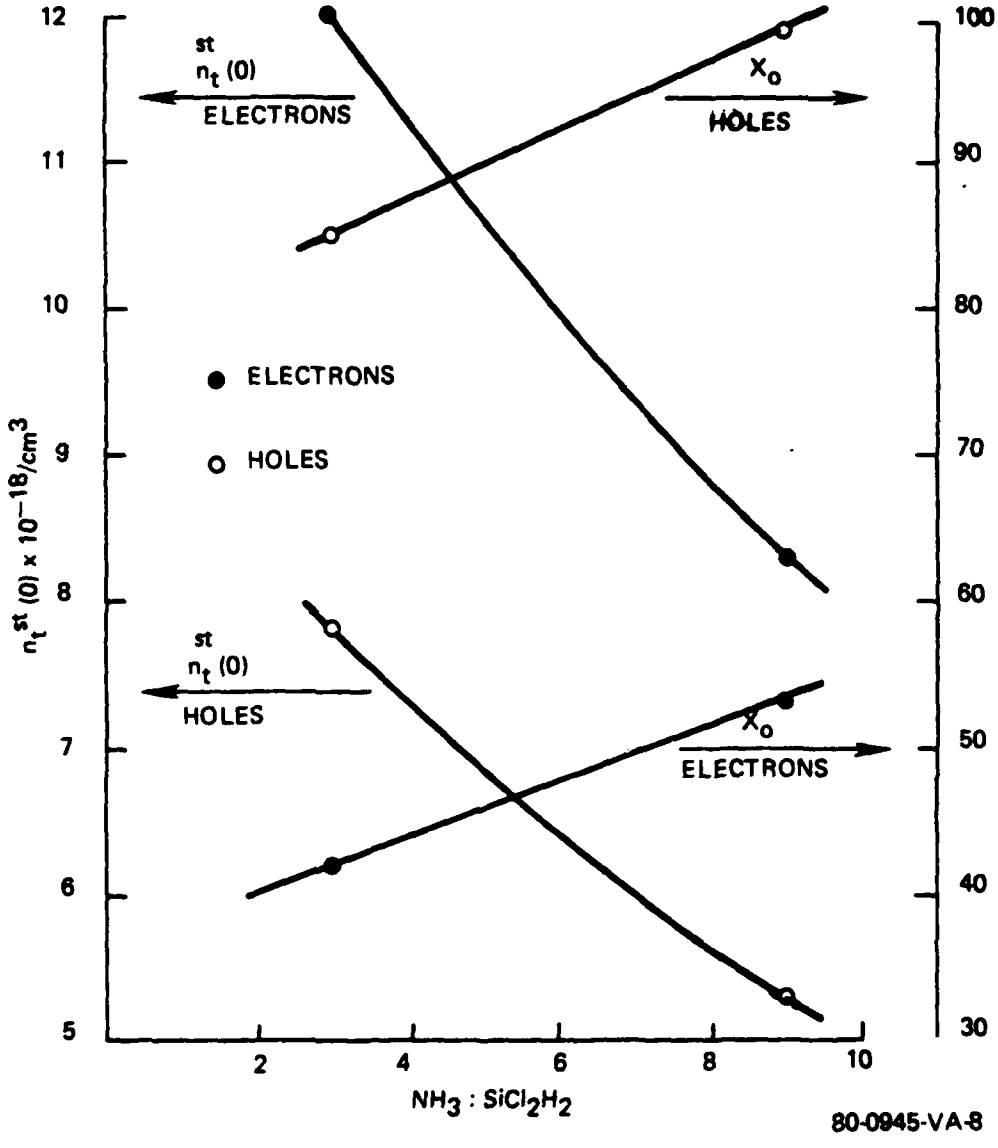


Figure 4-2. N^{st} (0) and X_o vs. NH_3:$SiCl_2$ ratio (LPCVD)

Table 4-1. Comparison of the density of trapped holes and electrons, n_t^{st}, trapping distance, X_o and cross section, for LPCVD and APCVD nitrides $T_{DEP}=750^{o}C$, $T_{MEAS}=25^{o}C$.

NITRIDE TYPE	APCVD				LPCVD	
$NH_3:SiH_4$ RATIO	28:1	150:1	300:1	450:1	9:1	3:1
CARRIER	HOLES	HOLES	HOLES	HOLES	HOLES	HOLES
$n_t^{st}(0) = N_t$ ($\#/cm^3$)	4.0	3.54	3.31	3.23×10^{18}	5.3	8.3×10^{18}
X_o (Å)	59	76	90	109	99	85
σ_t (cm^2)	4.23	3.71	3.35	2.84×10^{-13}	1.9	1.41×10^{-13}

NITRIDE TYPE	APCVD				LPCVD	
$NH_3:SiCl_2H_2$	28:1	150:1	300:1	450:1	9:1	3:1
CARRIER		ELECTRONS			ELECTRONS	
$n_t^{st}(0) = N_t$ ($\#/cm^3$)	4.73	4.38	4.09	4.02×10^{18}	8.3	12×10^{18}
X_o (Å)	25	43	63	79	53	42
σ_t (cm^2)	8.62	5.36	3.86	3.17×10^{-13}	2.27	1.98×10^{-13}

80-0945-VA-9

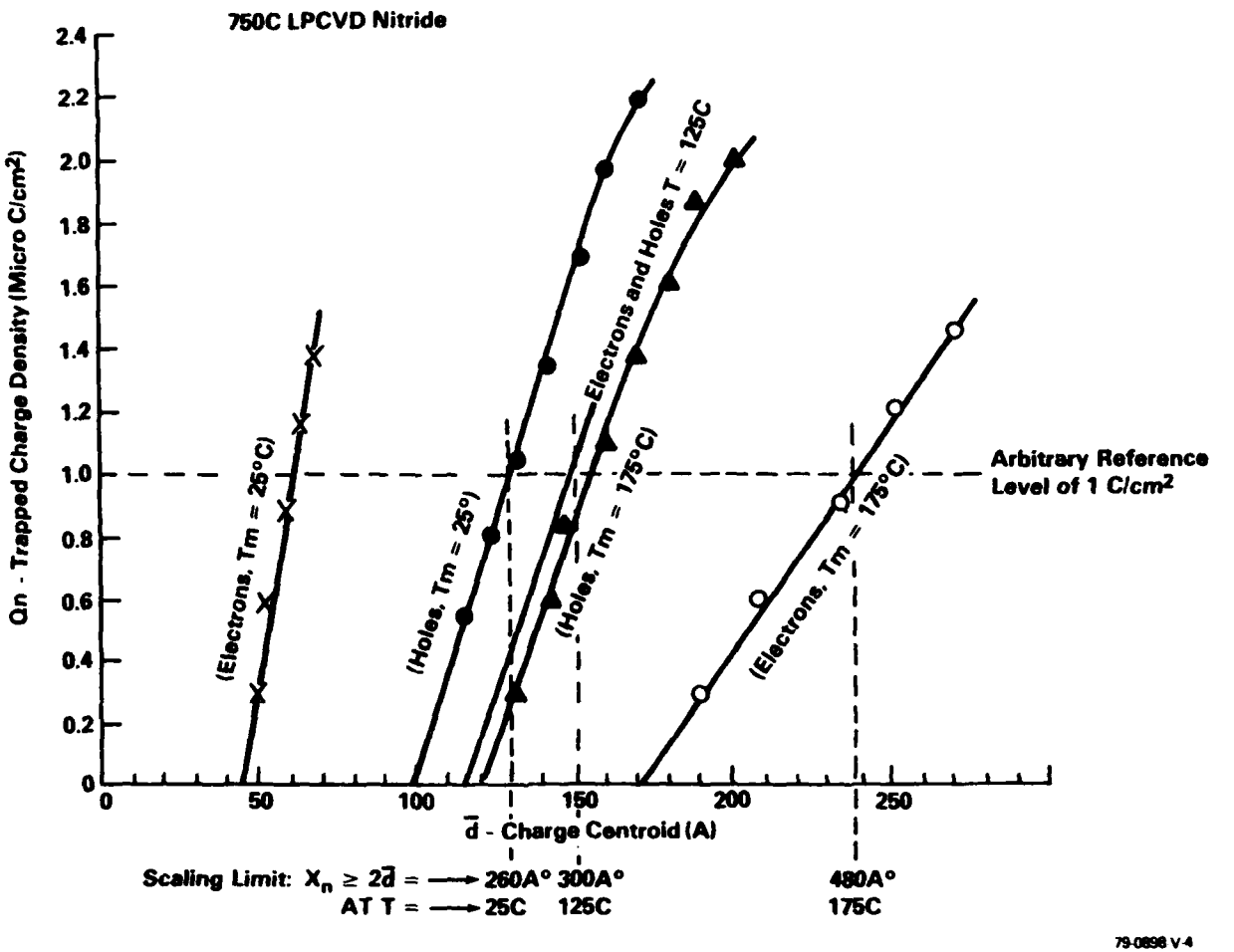


Figure 4-3. Trapped charge density vs charge centroid

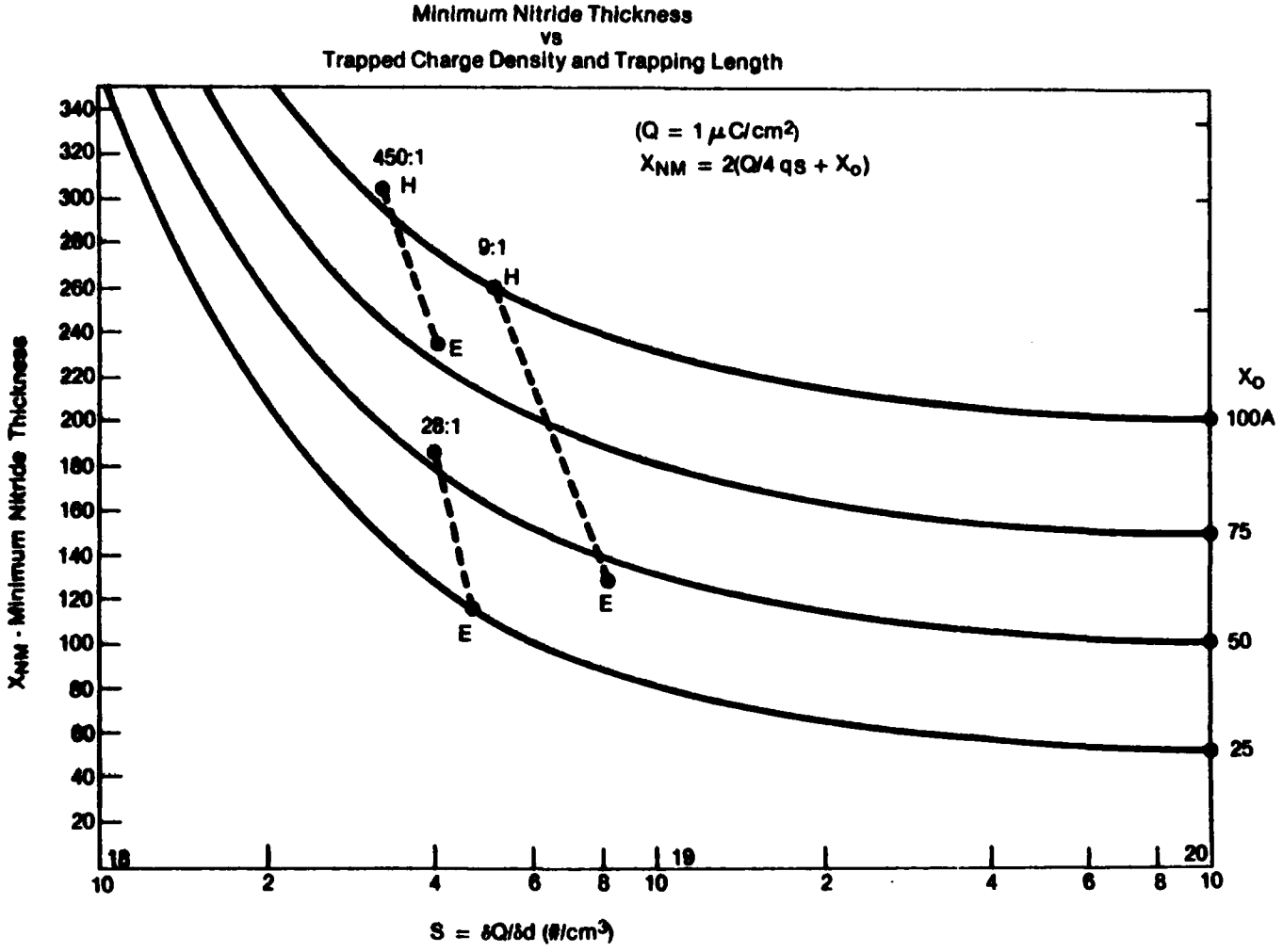


Figure 4-4. Minimum nitride thickness vs. trapped charge density and trapping length

$(2X_o)$ as the density of trapped charge, S, increases or the stored nitride charge, Q_n decrease.

4.2 D-C Memory Window and Non-Memory Threshold

The data summarized in Tables 4-2 thru 4-6 are the result of both polysilicon and metal gate capacitor structures fabricated on both bulk and SOS substrates. The data in Table 4-2 gives the ±20VDC memory window size for various memory nitride gate structures and post anneal treatments. Since the memory transistor is a Drain Source Protected Structure (DSP), the positive threshold value V_T^+ is an indication of the non-memory threshold voltage. The positive shift in both the threshold voltage and center of the memory window when the devices were post H_2 annealed suggest that the fixed positive charge in the nitride is being decreased. It is also observed that at the ±20V bias level the memory window is larger for the H_2 annealed devices for each of the gate structures. The temperature bias stability of the devices was obtained from capacitor C-V measurements. Table 4-3 shows the results for ±20V voltage bias and 200°C temperature stress for a N^- substrate structure while the results for a P^- substrate structure are shown in Table 4-4. It should be noted that the above data (Table 4-2 thru 4-4) are for metal gate devices fabricated in an SOS substrate. The polysilicon gate non-memory all oxide structure flatband and threshold voltage values, are shown in Table 4-5. The process variables included

Table 4-2. ±20V DC memory window, lot 4225

Wafer#	Thickness X1 + X2 = X_N	Treatment	Sample Size	V_T^+	V_T^-	ΔV_T
2	429A + 0 = 429A	2	8	−3.85	−9.48	5.68
3	429 + 0 = 429	1	15	−7.5	−11.58	4.08
5	143 + 244 = 387	1	20	−6.5	−10.50	4.00
7	143 + 244 = 387	2	8	−4.23	−8.78	4.55
9	0 + 374 = 374	2	18	−2.86	−7.74	4.88
12	0 + 374 = 374	1	13	−5.98	−9.45	3.47

V_T^- = −20V dc State, V_T^+ = +20V dc State

Nitrides Types

X1 - APCVD Nitride, NH_3:SiH_4 = 28:1
X2 - LPCVD Nitride, NH_3:SiH_4 = 9:1

Special Treatments and Anneals

1 - No Treatment
2 - Nitride Oxidized in Steam for 30 min at 900°C, Followed by a 900°C Anneal in H_2 for 60 min.

81-1025-V-31

Table 4-3. Temperature bias stress test N^- substrate capacitor structures from device lot #4225. Devices includes APCVD, LPCVD and APCVD + LPCVD films with X_n=425A, 374A, and 143 + 294A.

	APCVD NITRIDE (28:1, X_N = 429Å)	LPCVD NITRIDE (9:1, X_N = 374Å)	APCVD, 28:1 X_N = 143A LPCVD, 9:1 X_N = 244A
NITRIDE OXIDATION & H_2 ANNEAL FOR 60 MINUTES AT 900°C	WAFER 2 N^- GATE V_{FB} = -0.9 +20V = 0 -20V = 0.1	WAFER 9 N^- GATE V_{FB} = -0.6 +20V = 0 -20V = 0	WAFER 7 N^- GATE V_{FB} = -0.2 +20V = 0 -20V = 0.2
NO ANNEAL	WAFER 3 N^- GATE V_{FB} = -1.9 +20V = 0 -20V = 0	WAFER 12 N^- GATE V_{FB} = -2.0 +20V = 0 -20V = 0	WAFER 5 N^- GATE V_{FB} = -1.9 +20V = 0 -20V = 0

STRESS TEMPERATURE 200°C

80-0945-VA-10

Table 4-4. Temperature bias stress test for P^- substrates capacitor structures from device lot #4225. Devices includes APCVD, LPCVD and APCVD + LPCVD films with X_n=429A, 374A and 143 + 244A respectively.

	APCVD NITRIDE (28:1, X_N = 429Å)	LPCVD NITRIDE (9:1, X_N = 374Å)	APCVD/28:1 X_N = 143A LPCVD, 9:1 X_N = 244A
NITRIDE OXIDATION & H_2 ANNEAL FOR 60 MINUTES AT 900°C	WAFER 2 P^- GATE V_{FB} = 2.1 +20V = 0 -20V = 0.2	WAFER 9 P^- GATE V_{FB} = 2.5 +20V = 0.2 -20V = 0	WAFER 7 P^- GATE V_{FB} = 2.9 +20V = 0 -20V = 0
NO ANNEAL	WAFER 3 P^- GATE V_{FB} = -3.4 +20V =0 -20V = 0	WAFER 12 P^- GATE V_{FB} = -4.1 +20V = 0.05 -20V = 0	WAFER 5 P^- GATE V_{FB} = -3.9 +20V = 0.3 -20V = 0

STRESS TEMPERATURE 200°C

80-0945-VA-11

Table 4-5. Variation in flatband voltage and threshold voltage as a function of doping procedures and time for polysilicon before memory nitride process.

DOPING SOURCE / POLYSILICON THICKNESS	PHOSPHINE 900°C, 15 MIN	DOPED GLASS 900°C, 40 MIN	DOPED GLASS 900°C, 25 MIN
3.6K Å	WAFER 1 V_{FB} = -1.15 V_T = -1.8	WAFER 3 V_{FB} = -0.85 V_T = -1.39	WAFER 5 V_{FB} = 0.77 V_T = -1.38
5.8K Å	WAFER 7 V_{FB} = -1.54 V_T = -2.17	WAFER 9 V_{FB} = -1.29 V_T = -2.07	WAFER 11 V_{FB} = -1.10 V_T = -2.00

X_{OX} = 822 Å, SAMPLE SIZE = 5

80-0945-VA-12

polysilicon thickness, doping source and doping times. The results tend to suggest that for the 3.6KA polysilicon layer, a small amount of phosphorous could be tailing into the oxide. Non-memory threshold voltage data and ±20V memory window sizes data in Table 4-6 are given for the polysilicon gate over oxidized nitride . It was observed that oxidizing for 60 minutes as opposed to 30 minutes did not appear to have any significant effect.

4.3 Pulse Response of Capacitor Structures

The curves presented in this section describes the pulse response of capacitor structures for electron injection. The devices were fabricated on n-type silicon without a means to contact the p-type inversion layer, disallowing pulsing with a negative polarity or hole injection. The flatband voltage shift, V_{FB}, produced by a lusec pulse as a function of NH_3:SiH_4 ratio for various field levels are shown in Figure 4-5. In Figure 4-6, V_{FB} is shown as a function of pulse width for a NH_3:SiH_4 ratio of 150:1 and a NH_3:SiH_4 ratio of 28:1 in Figure 4-7. The pulse response of the two step nitride consisting of a 102A (28:1 APCVD) + 401A (9:1 LPCVD) and 172A (28:1 APCVD) + 299A (9:1 LPCVD) are shown as a function of pulse width for various nitride fields in Figures 4-8 and 4-9 respectively. Figures 4-10 and 4-11 shows the pulse response of a 200A (3:1 LPCVD) + 102A (9:1 LPCVD) and a 200A (3:1 LPCVD) + 204A (9:1 LPCVD) film respectively. The

Table 4-6. Memory gate and fixed threshold devices polysilicon gate over oxidized nitride.

WAFER NO. 2*			
V^{+}_{TM}	V^{-}_{TM}	V_{YM}	V_{TF}
−3.93	−10.62	14.55	−1.05

WAFER NO. 3**			
−4.08	−10.63	15.43	−1.24

SAMPLE SIZE = 3

THE GATE OF THE FIXED THRESHOLD DEVICE CONSIST OF A NITRIDE/OXIDE STRUCTURE WITH X_o = 875 A AND X_N = 499 A

* OXIDIZED NITRIDE FOR 30 MIN IN STEAM AT 900°C

** OXIDIZED NITRIDE FOR 60 MIN IN STEAM AT 900°C

V^{+}_{TM} -- +20 V DC STATE

V^{-}_{TM} -- −20V DC STATE

80-0945-VA-13

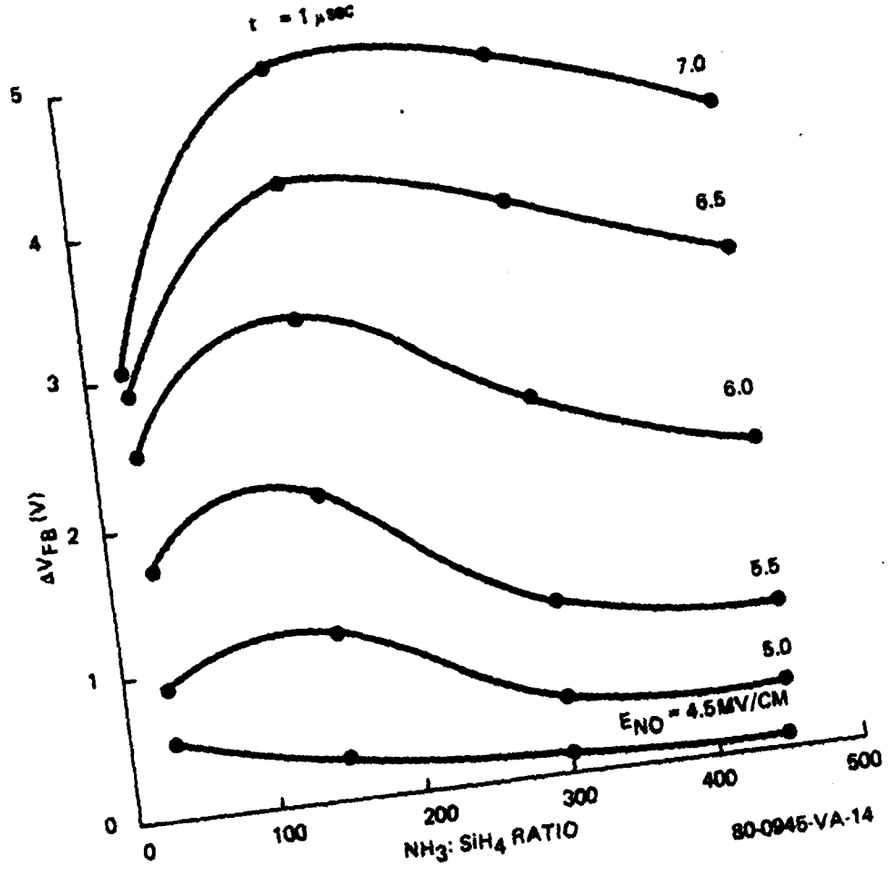


Figure 4-5. Flatband voltage vs. NH_3:SiH_4 ratio

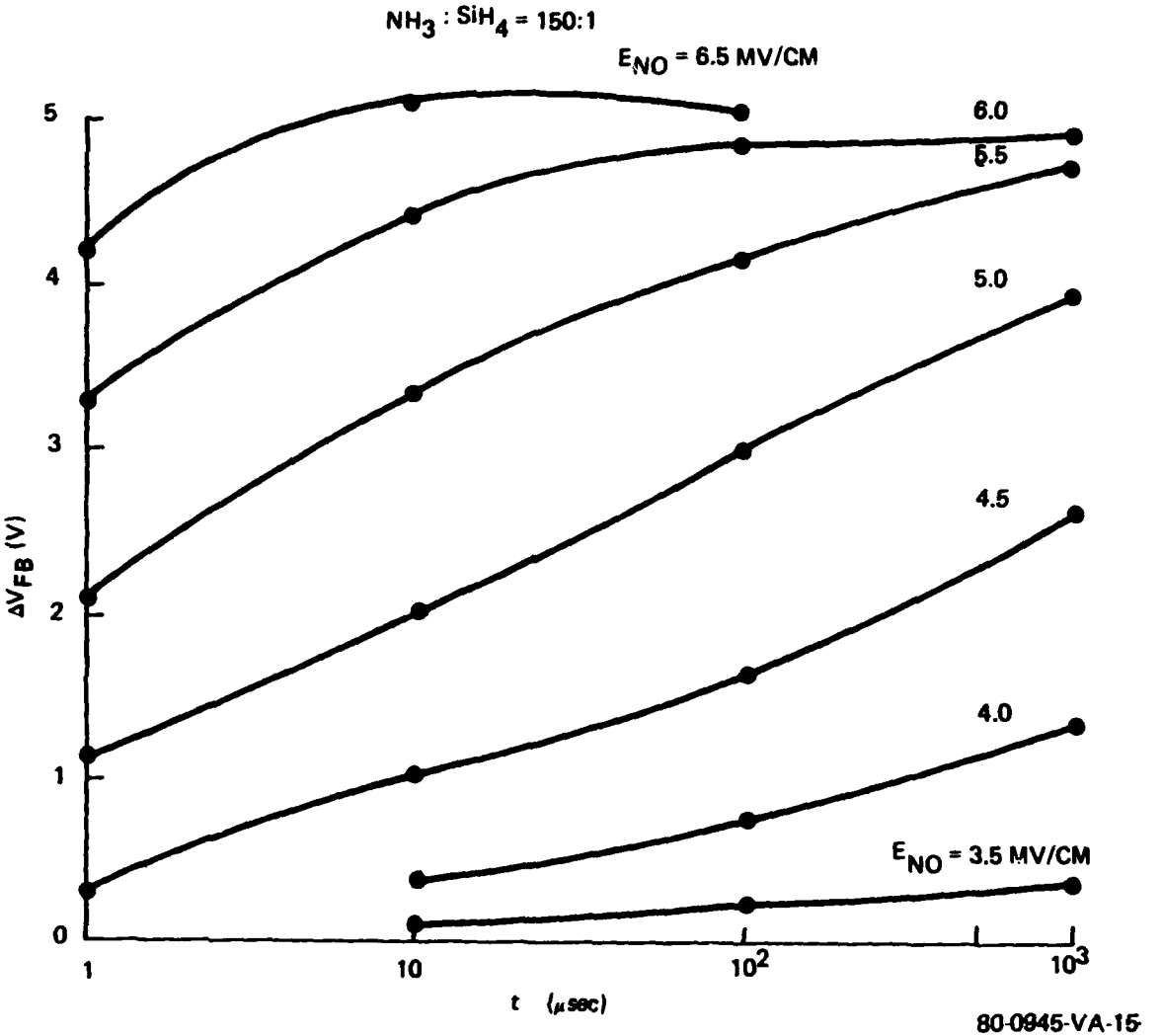


Figure 4-6. Flatband voltage vs. pulse width single APCVD nitride with NH_3:SiH_4=150:1

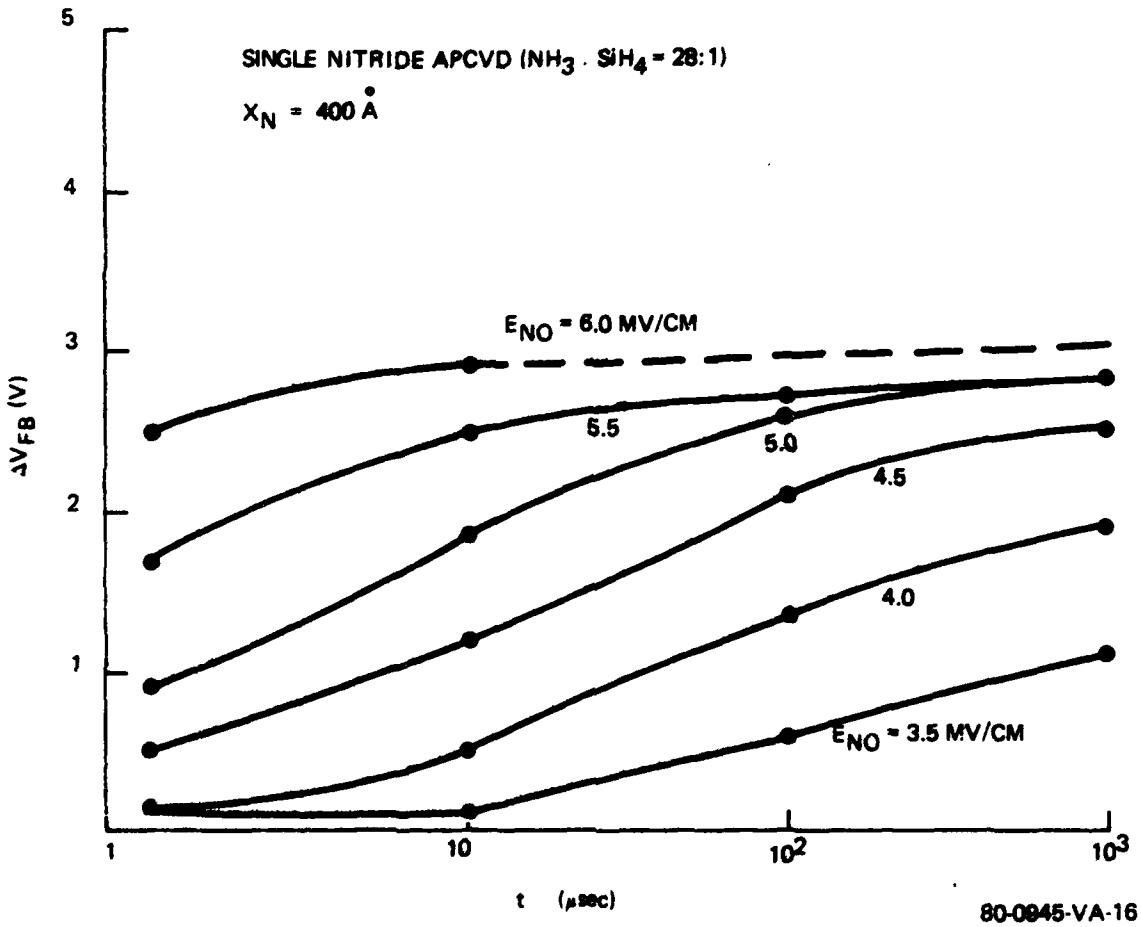


Figure 4-7. Flatband voltage vs. pulse width single APCVD nitride with NH_3:SiH_4 = 28:1, X_N = 400A

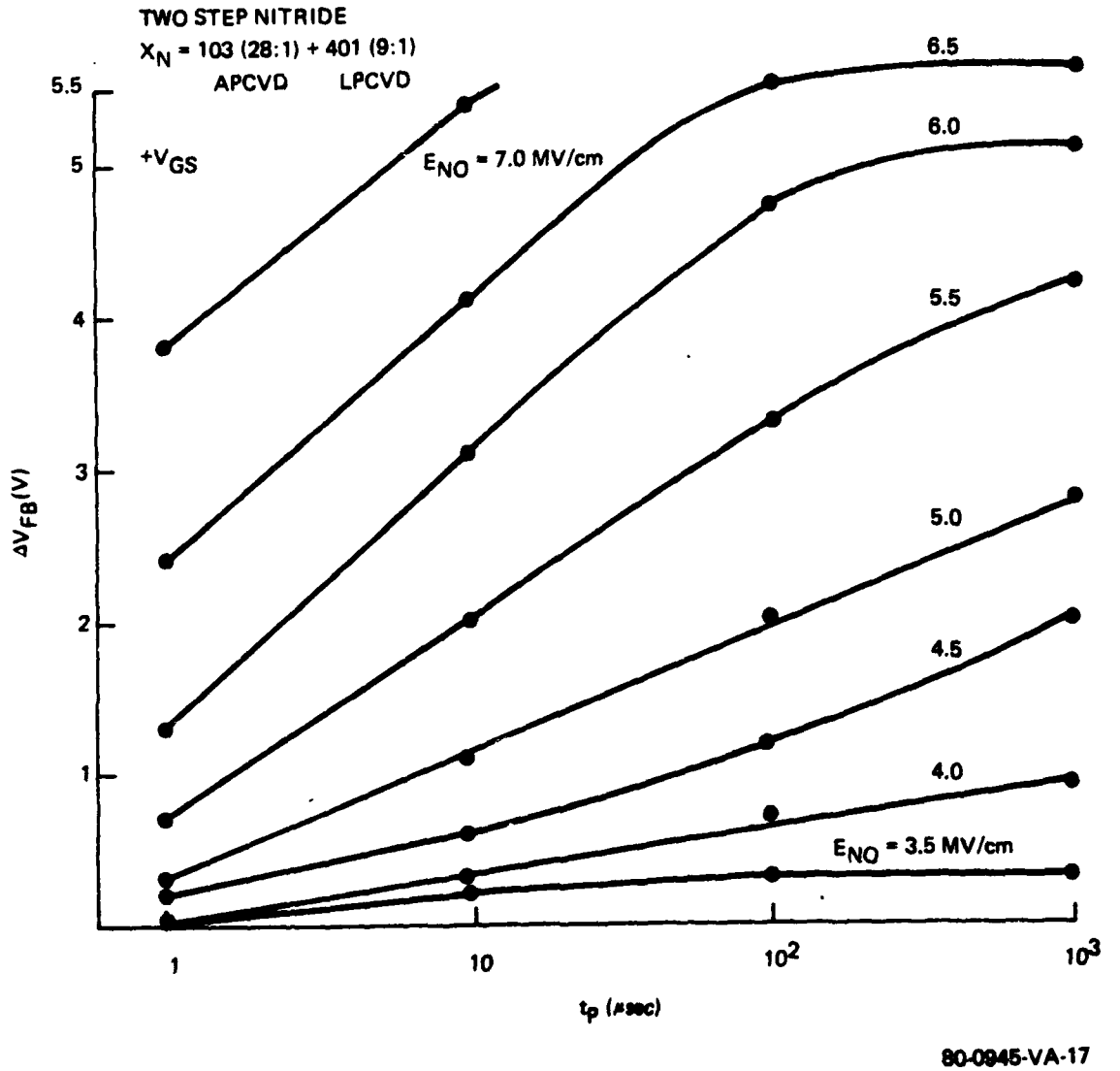


Figure 4-8. Flatband voltage vs. pulse width. Two step nitride, APCVD (NH_3:SiH_4=28:L) + LPCVD (NH_3:$SiCl_2H_2$=9:1), X_N = 103A + 401A

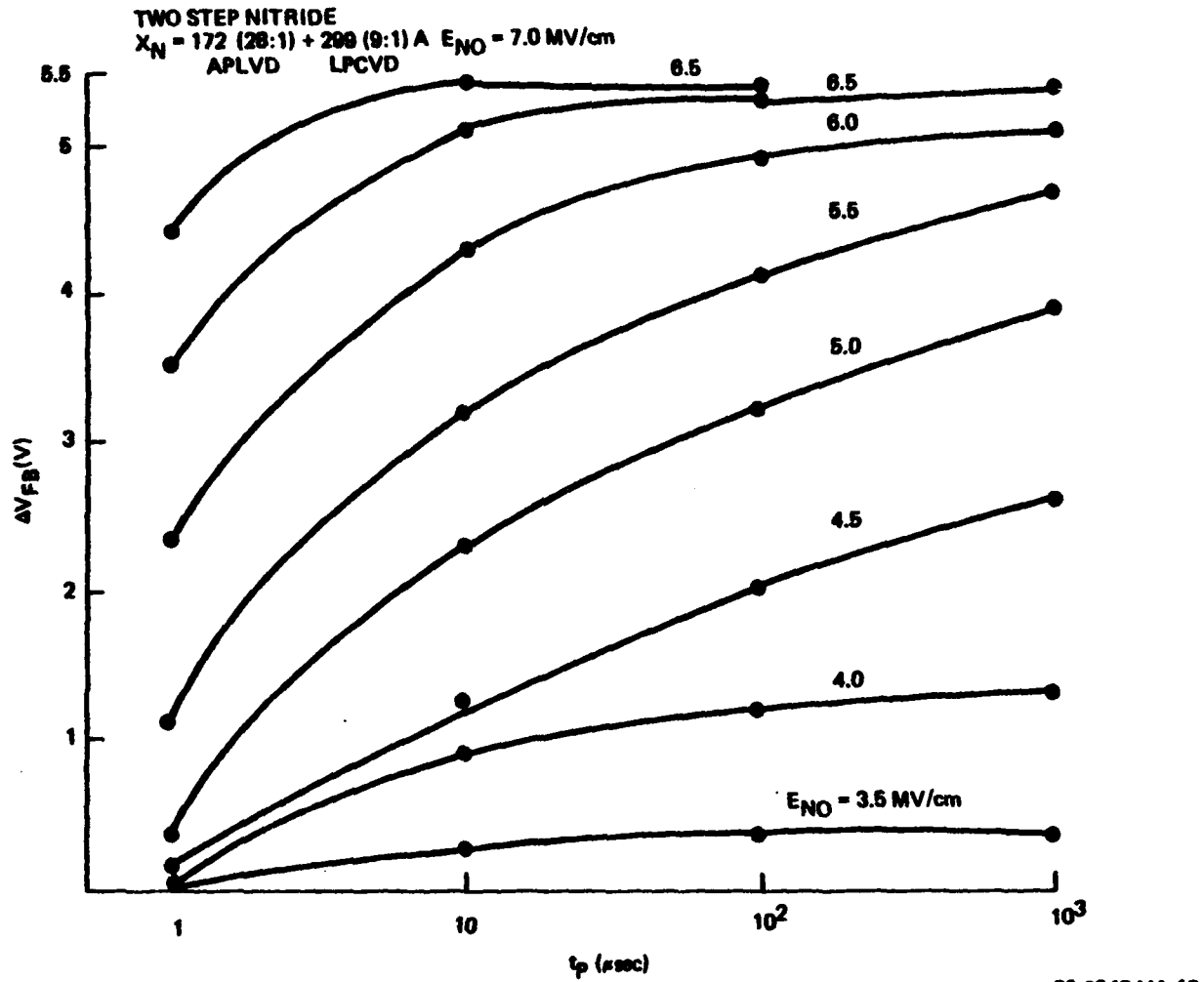


Figure 4-9. Flatband voltage vs. pulse width. Two step nitride, APCVD (NH_3:SiH_4 = 28:1) + LPCVD (NH_3:$SiCl_2H_2$ = (9:1), X_n = 172 + 299A

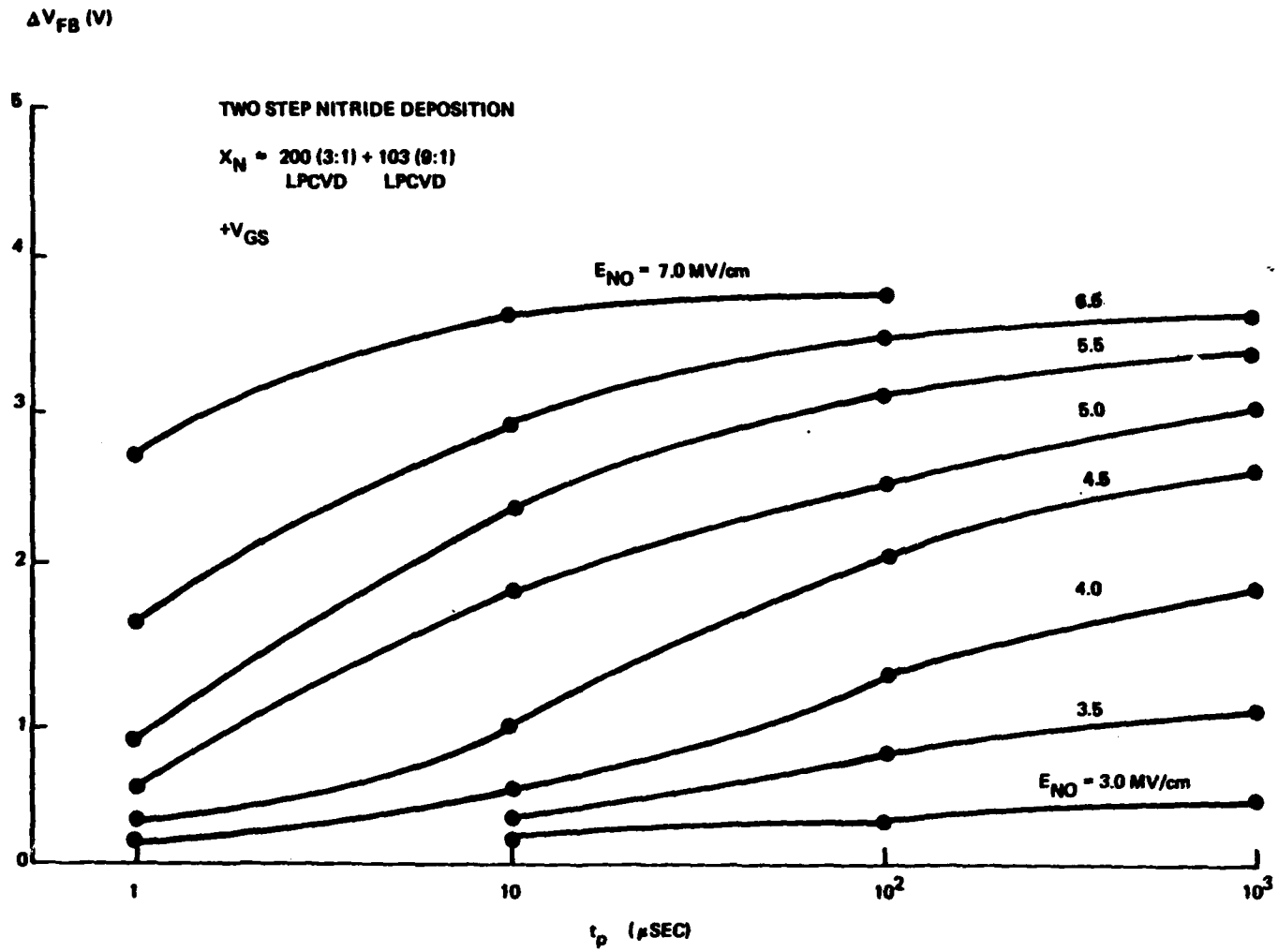


Figure 4-10. Flatband voltage vs. pulse width. Two step LPCVD nitride. X_n = 200A (NH_3:$SiCl_2H_2$ = 3:1) +103A (NH_3:$SiCl_2H_2$=9:1)

80-0945-VA-19

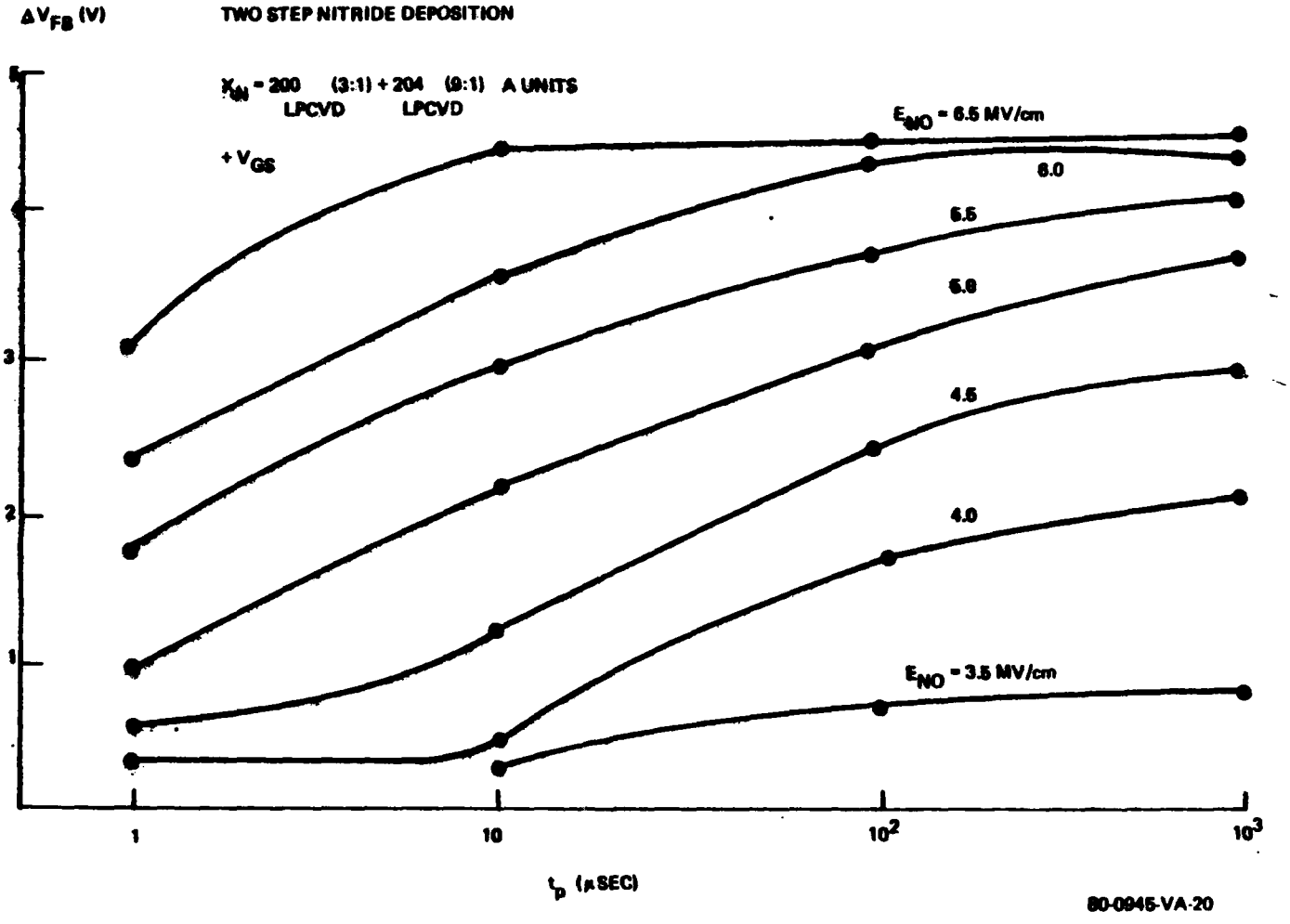


Figure 4-11. Flatband voltage vs. pulse width. Two step LPCVD nitride. 200Å (NH_3:$SiCl_2H_2$ = 3:1) +204Å (NH_3:$SiCl_2H_2$ = 9:1)

pulse response is larger for the low conductive film, NH_3:SiH_4 = 28:1 (APCVD) for fields of 4.5 MV/cm (single nitride structure). The low value of flatband shift at which the 28:1 film saturates is attributed to detrapping at the leading edge of the charge centroid because of the relative high conductivity of the film. The optimum NH_3:SiH_3 ratio for a single APCVD nitride occurs between 28:1 and 450:1 for a 1usec pulse with amplitude 4.5 MV/cm. The heat treatment history in Table 4-7 gives the process variables of devices represented by the data presented in Figure 4-12 thru 4-14. In Figure 4-12 the flatband shift is shown as a function of post anneal treatment for a 1usec pulse and initial nitride field. The results for a 10usec pulse are shown in Figure 4-13 while Figure 4-14 depicts the behavior for a 100usec pulse width. The structures revealed that a larger pulse response was obtained for the device where the 51A layer nitride was annealed in N_2. The nitride containing the 29A layer that was annealed in H_2 showed the slowest pulse responses when both nitride layers were annealed in H_2. A positive shift in both the threshold or flatband voltage and the center of the memory window was observed again, suggesting a decrease in the fixed positive charge in the film.

4.4 Conductance and Retention Results

The relative conductance - voltage peak heights for the capacitor structures that contained the 29A and 51A thin

Table 4-7. Heat treatment history received by the thin nitride X_n=29A and 51A. The 391A film received a high temperature heat treatment only in columns B and F.

ANNEAL AMBIENT / X_N	H_2 @ 900°C	H_2 @ 900°C + POST H_2 @ 900°C	N_2 @ 900°C	NH_3 @ 1100°C
X_{N1} = 29 A X_{N2} = 391 A	COLUMN A	COLUMN B	COLUMN C	COLUMN D
X_{N1} = 51 A X_{N2} = 391 A	COLUMN E	COLUMN F	COLUMN G	COLUMN H

80-0945-VA-21

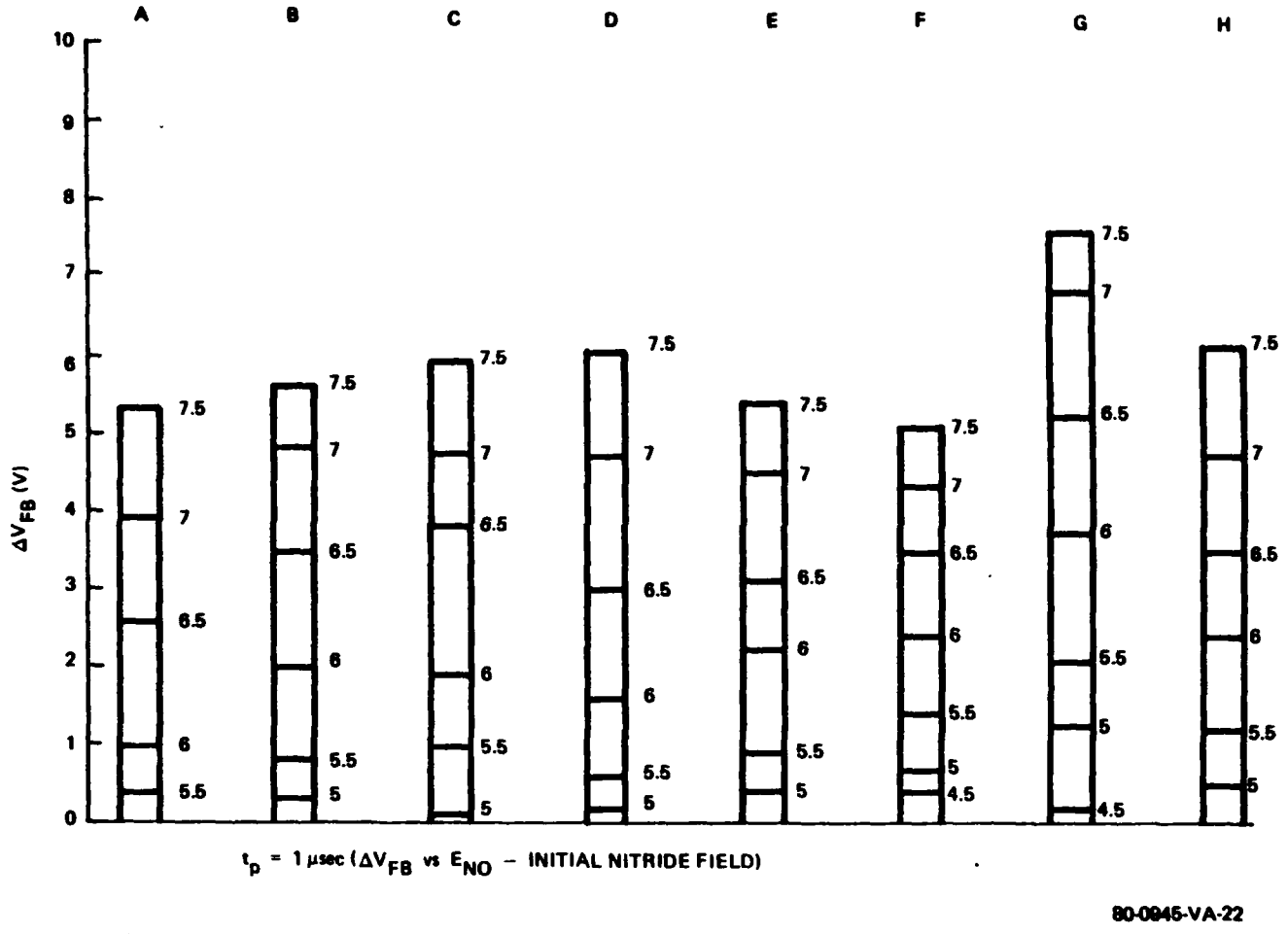


Figure 4-12. Memory pulse response vs. nitride anneal. Pulse width; t_w = 1μsec. Two step LPCVD nitride. X_n=29+391A and 51 + 391A. NH_3:$SiCl_2H_2$=3:1

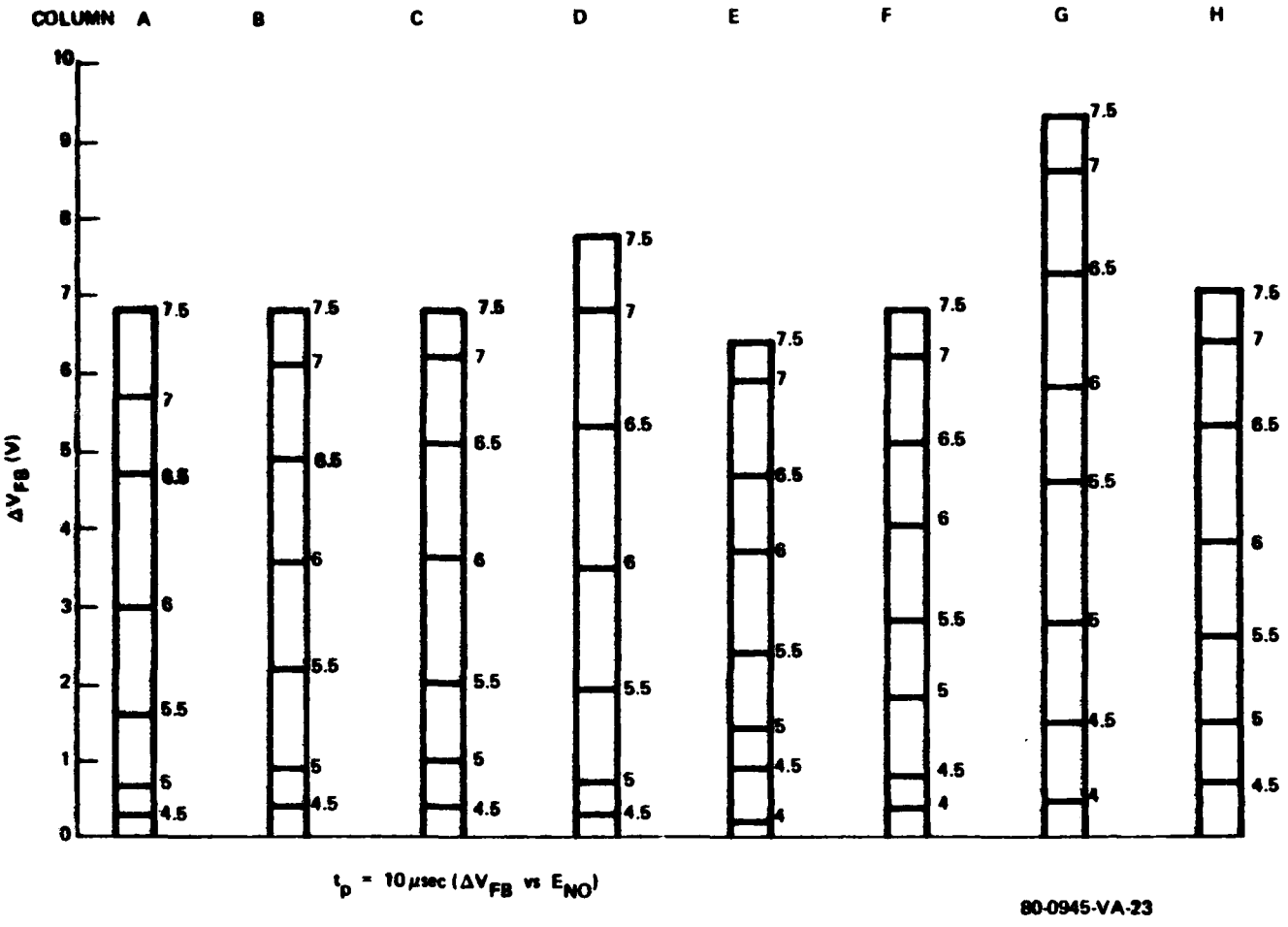


Figure 4-13. Memory pulse response vs. nitride anneal ambient. Pulse width, t_w= 10μsec. Two step LPCVD nitride X_n=29+391A and 51+391A. NH_3:$SiCl_2H_2$=9:1

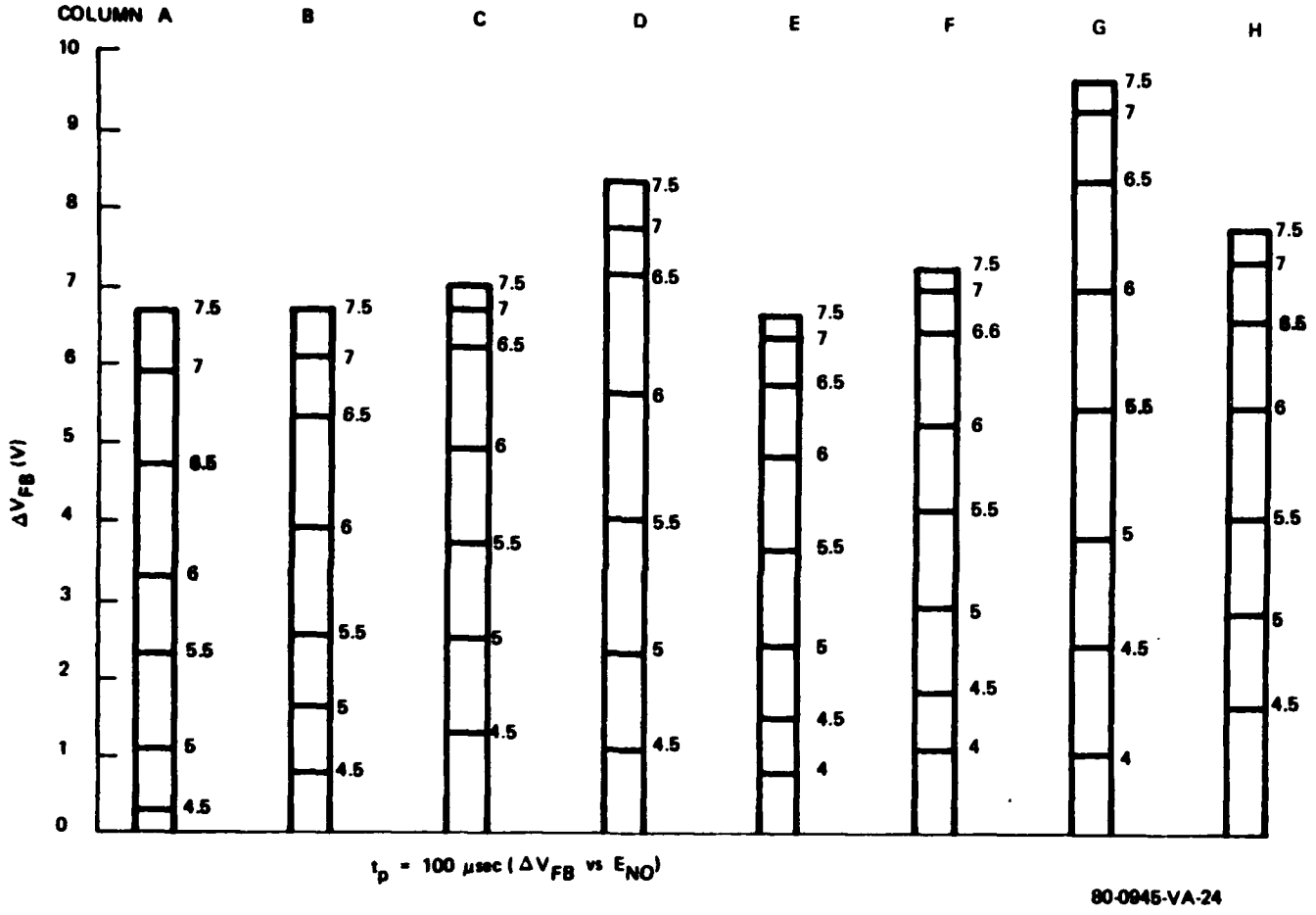


Figure 4-14. Memory pulse response vs. nitride anneal ambient. Pulse width, t_w=100μsec. Two step LPCVD nitride X_n= 29+391A and 51+391A. NH_3:$SiCl_2H_2$=9:1

film over which 391A layer nitride was deposited (LPCVD with various post anneal treatments) are shown in Table 4-8. In Table 4-9, the electron and hole decay rates are presented. The structures that had the thin nitride films annealed in NH_3 had the smallest relative peak height, suggesting that these structures treated as such have the lowest interface state density. The charge decay was found to be lowest for the 29A layers that were annealed in NH_3. The curves in Figure 4-15 and 4-16 shows the capacitance - voltage and conductance - voltage relationship for an SOS memory capacitor structure from a 6023T test pattern. The major variations observed in the unstressed device and a device that was stressed for 1 hour at 28V was a significant peak growth of the conductance peak of the stressed device when compared to the initial characteristics.

4.5 Endurance Cycling, Retention and Pulse Response for MNOS/SOS Memory Transistor

The wave shapes shown in Figure 4-17 are the stress cycle waveforms used to endurance cycle the devices. The curves in figure 4-18 gives the $\pm$20V DC memory threshold voltage as a function of endurance cycles for a 100usec pulse and an electric field stress of 5 MV/cm, for a memory gate dielectric structure consisting of a 374A LPCVD nitride. The one structure labeled annealed was post nitride annealed in H_2 for 30 min. at 900^{o}C. The $\pm$20V memory window size is

Table 4-8. Conductance - voltage relative peak heights, lot #01. Two step LPCVD nitride. X_n=29A and 391A 51 + 391A. NH_3:$SiCl_2H_2$=9:1.

ANNEAL AMBIENT / X_N	H_2 @ 900°C	H_2 @ 900°C + POST H_2 @ 900°C	N_2 @ 900°C	NH_3 @ 900°C	NH_3 @ 1100°C
X_{N1} = 29 A X_{N2} = 391 A	0.9	1.00	0.83	0.38	0.25
X_{N1} = 51 A X_{N2} = 391 A	0.6	1.00	0.43	0.36	0.30

THE CONDUCTANCE PEAK HEIGHT OF THE CONTROL SAMPLE WAS USED AS THE REFERENCE

80-0945-VA-26

Table 4-9. Electron and hole decay rates, lot #01. Two step $NH_3:SiCl_2H_2$=9:1.

ANNEAL AMBIENT / X_N	H_2 @ 900°C	H_2 @ 900°C + POST H_2 @ 900°C	N_2 @ 900°C	NH_3 @ 900°C	NH_3 @ 1100°C
X_{N1} = 29 A X_{N2} = 391 A	ELECTRONS 0.55 HOLES 0.55	ELECTRONS 0.60 HOLES 0.50	ELECTRONS 0.55 HOLES 0.60	ELECTRONS 0.45 HOLES 0.30	ELECTRONS 0.40 HOLES 0.30
X_{N1} = 51 A X_{N2} = 391 A	ELECTRONS 0.55 HOLES 0.55	ELECTRONS 0.60 HOLES 0.60	ELECTRONS 0.60 HOLES 0.60	ELECTRONS 0.60 HOLES 0.50	ELECTRONS 0.60 HOLES 0.60

DECAY RATES IN VOLTS/DECADE

80-0945-VA-27

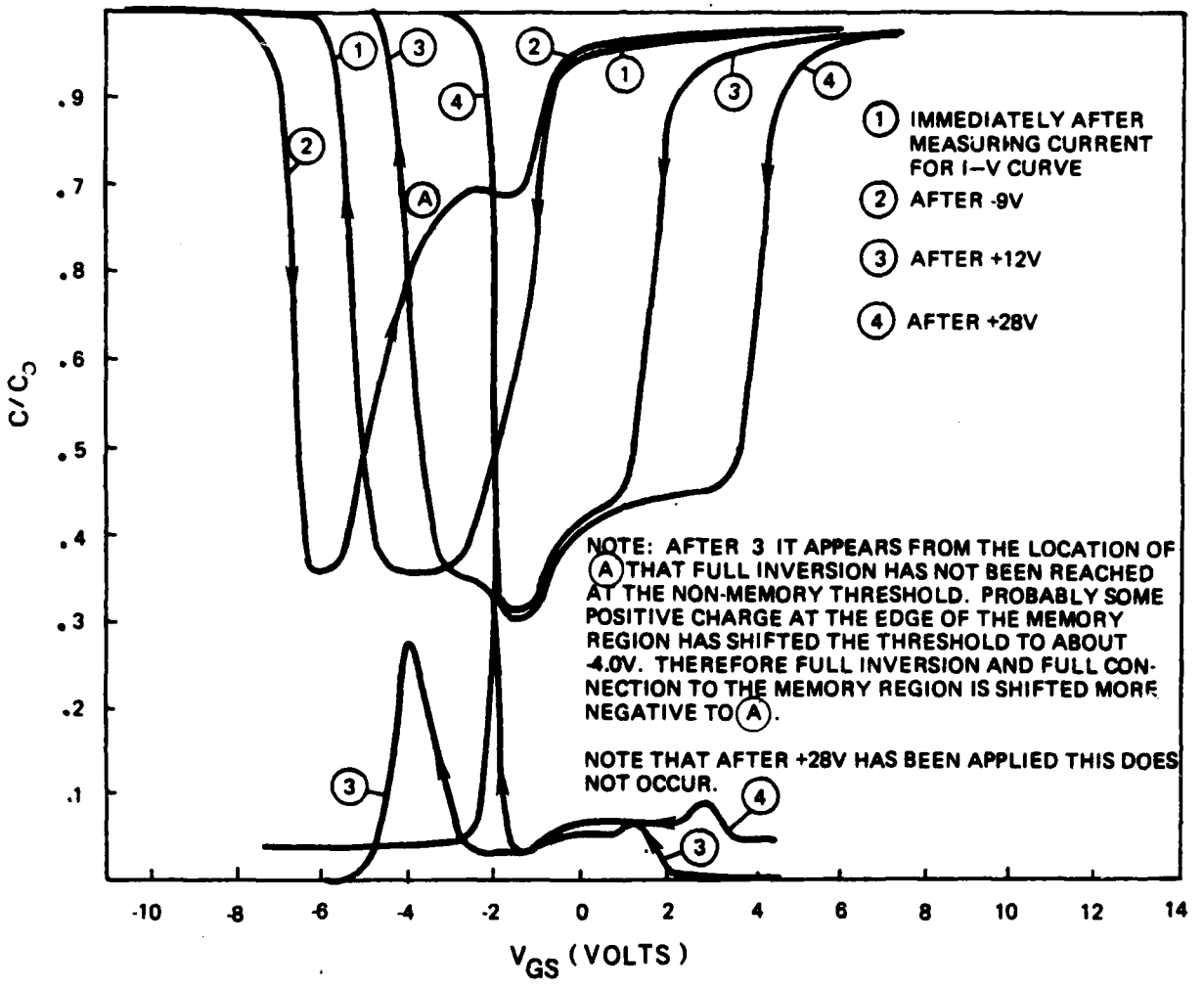


Figure 4-15. Capacitance-voltage and conductance-voltage curve before and after bias stress. Capacitor structures fabricated using MNOS/SOS process sequence.

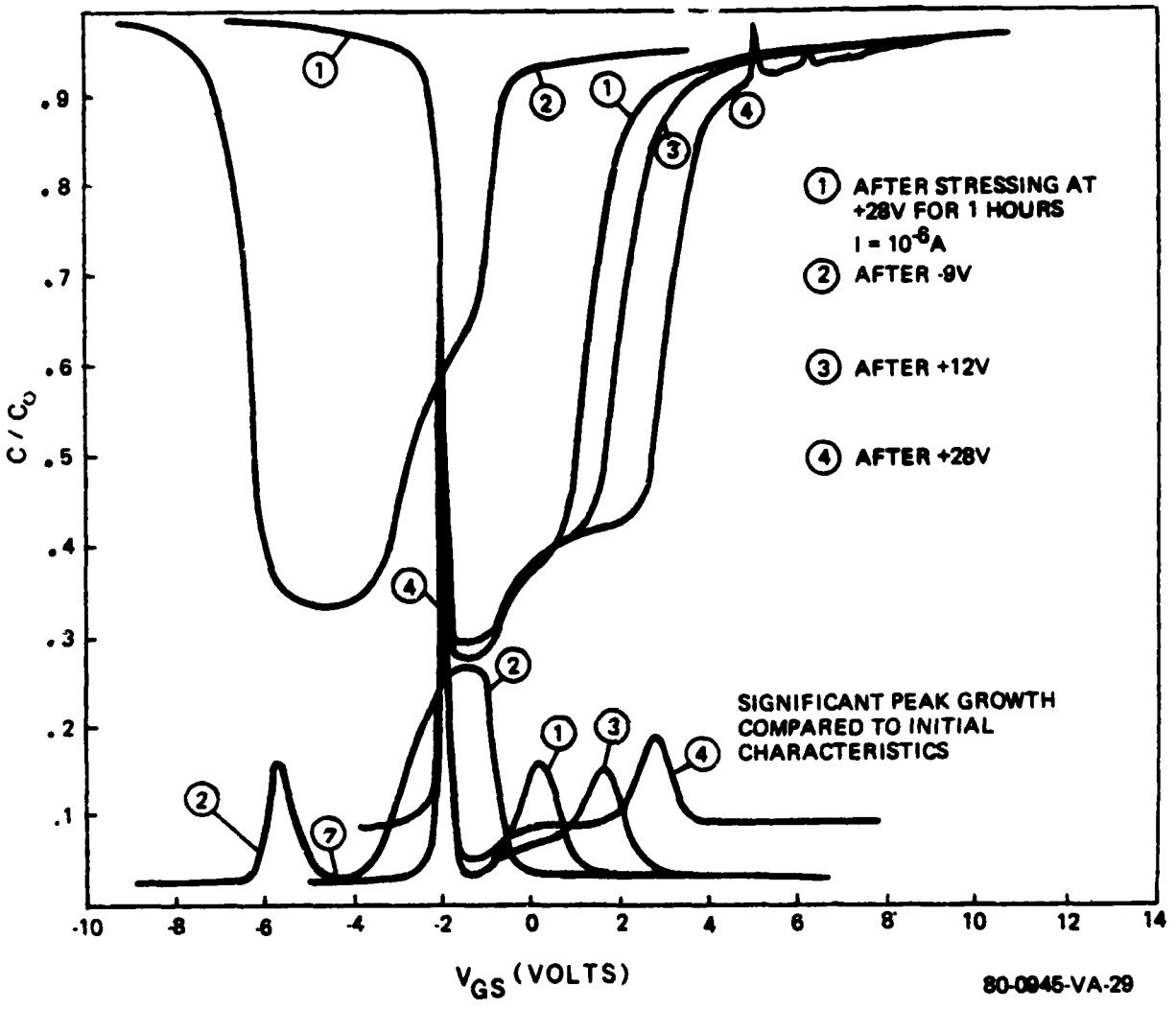


Figure 4-16. Capacitance-voltage and conductance-voltage curves after bias stressing. Capacitor structures fabricated with a MNOS/SOS process sequence.

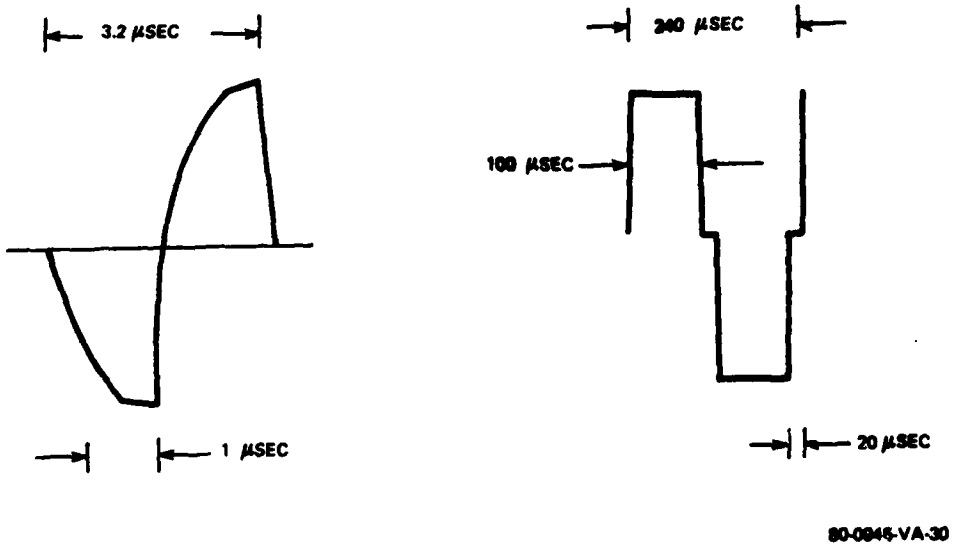


Figure 4-17. Stress cycle waveforms used for endurance stressing

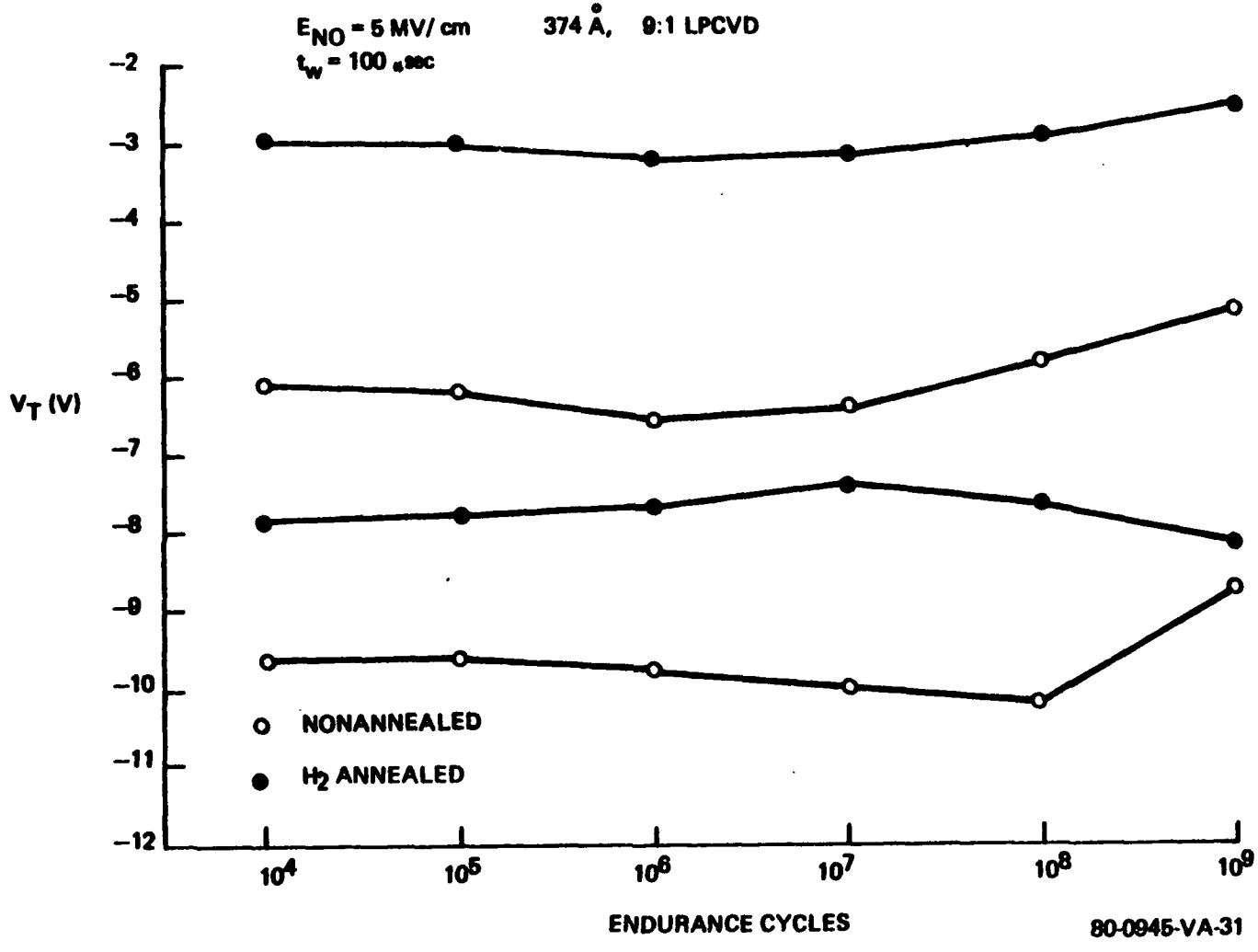


Figure 4-18. ±20V DC-window vs. endurance cycles, for devices annealed in H_2 and non-annealed structures. Pulse width, t_w = 100usec. X_n = 374A

shown as a function of endurance cycles in Figure 4-19, with the decay rates given after 10^9 cycles in Figure 4-20. The $\pm$20V DC memory threshold voltage level for a lusec pulse and an initial nitride field of 6 MV/cm for the same gate structures are given in Figure 4-21. The $\pm$20V DC memory window vs endurance cycles are shown in Figure 4-22. The initial voltage decay rate and the voltage decay rate after 10^{11} cycles are shown in Figures 4-23 and 4-24 for the non-annealed and H_2 annealed devices respectively. The results of a two step nitride structure consisting of a 143A (28:1 APCVD) + 244A (9:1 LPCVD) film are given in Figures 4-25 thru 4-29. The memory threshold voltage levels are shown as a function of endurance cycles for non-annealed and annealed devices are shown in Figure 4-25. In 4-26 the memory window size is depicted as a function of endurance cycles. The data retention in shown in Figure 4-27 and 4-28 for the unstressed structures and for the devices stressed to 10^{11} cycles respectively, while the voltage decay rate is shown as a function at endurance cycles in Figure 4-29 for devices that were annealed in H_2 and those structures that were not annealed. Note that the pulse memory windows and voltage decay rates were obtained for a pulse width of 100usec and a pulse amplitude of $\pm$27V. The curves in Figure 4-30 show the pulse memory window response and data retention of a +27, - 29 volt lusec pulse for the device structures that were stressed at 6 MV/cm with a pulse of lusec for 10^{11} cycles. In Figure 4-31 thru 4-34 the pulse response and data retention results are given for 374A (9:1 LPCVD) nitride

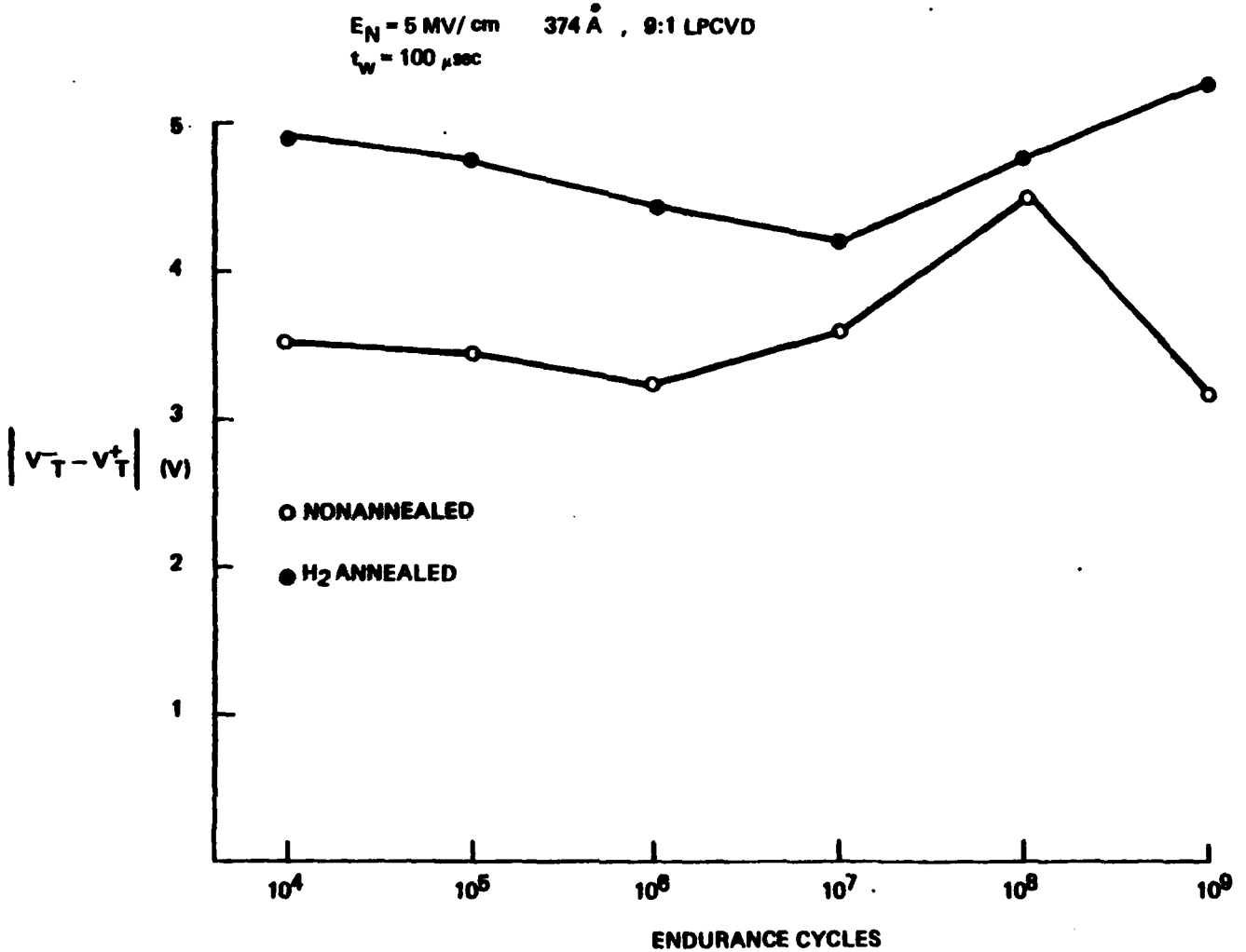


Figure 4-19. ±20V DC-window vs. endurance cycles for devices annealed in H_2 and non-annealed structures. Pulse width t_w= 100μsec. X_n = 374A

80-0945-VA-32

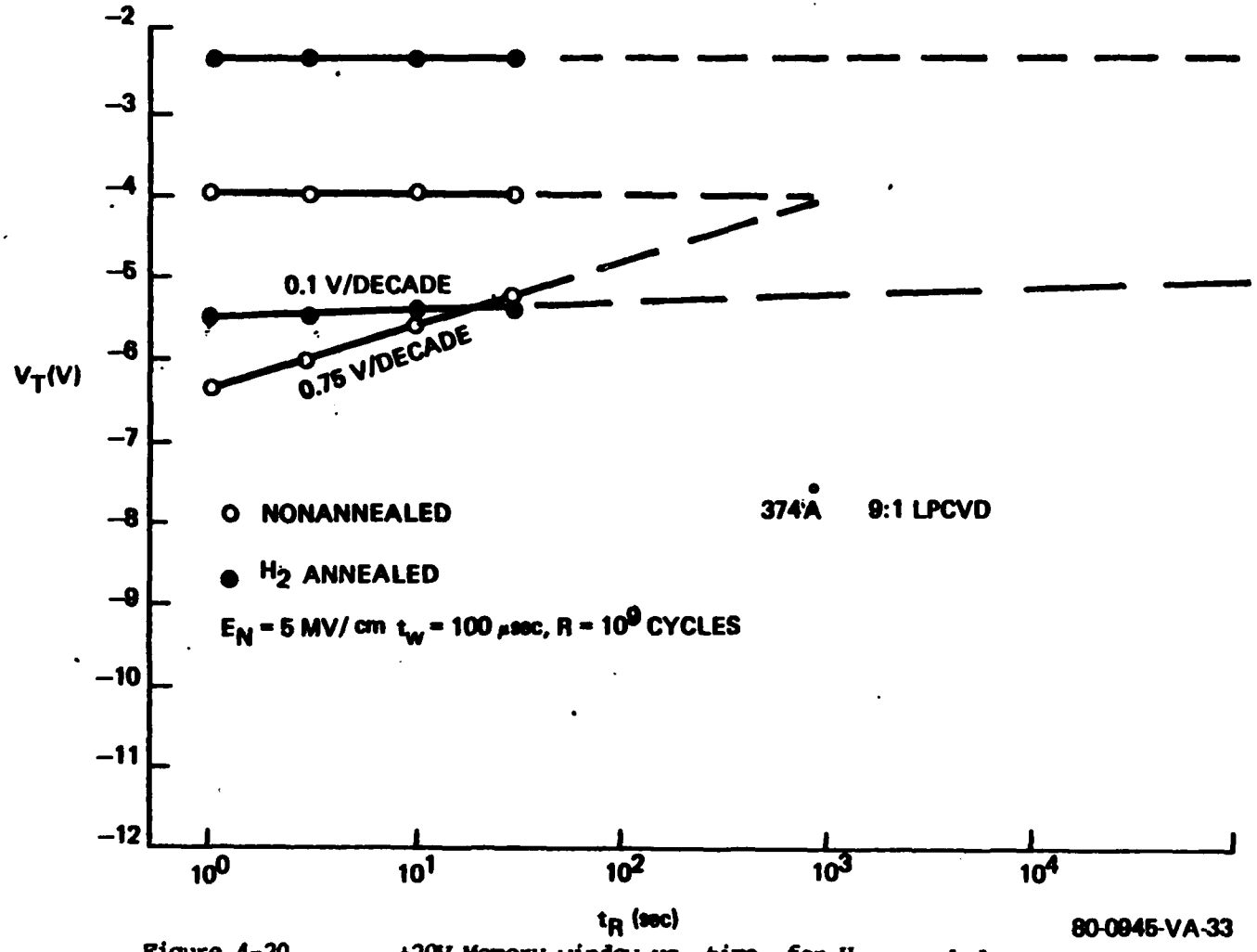


Figure 4-20. ±20V Memory window vs. time. for H_2 annealed and non-annealed devices after 10^9 endurance cycles. Pulse width, t_w=100μsec, E_n = 5MV/cm

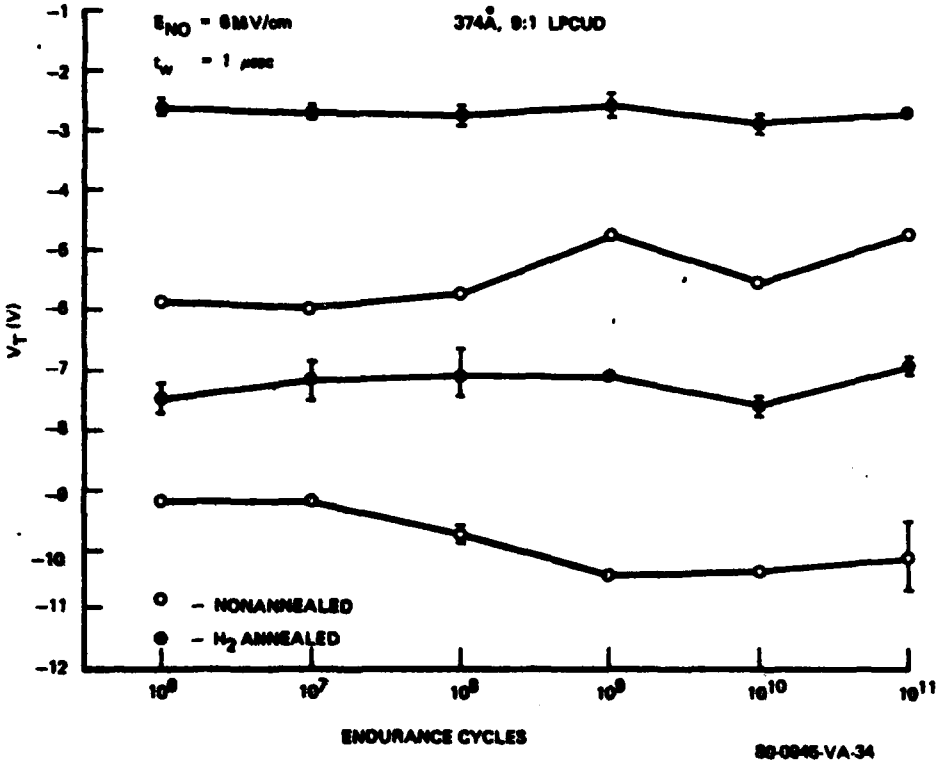


Figure 4-21. ±20V DC-window vs. endurance cycles, for H_2 annealed and non-annealed devices. Pulse width, t_w=1μsec, E_n = 6MV/cm

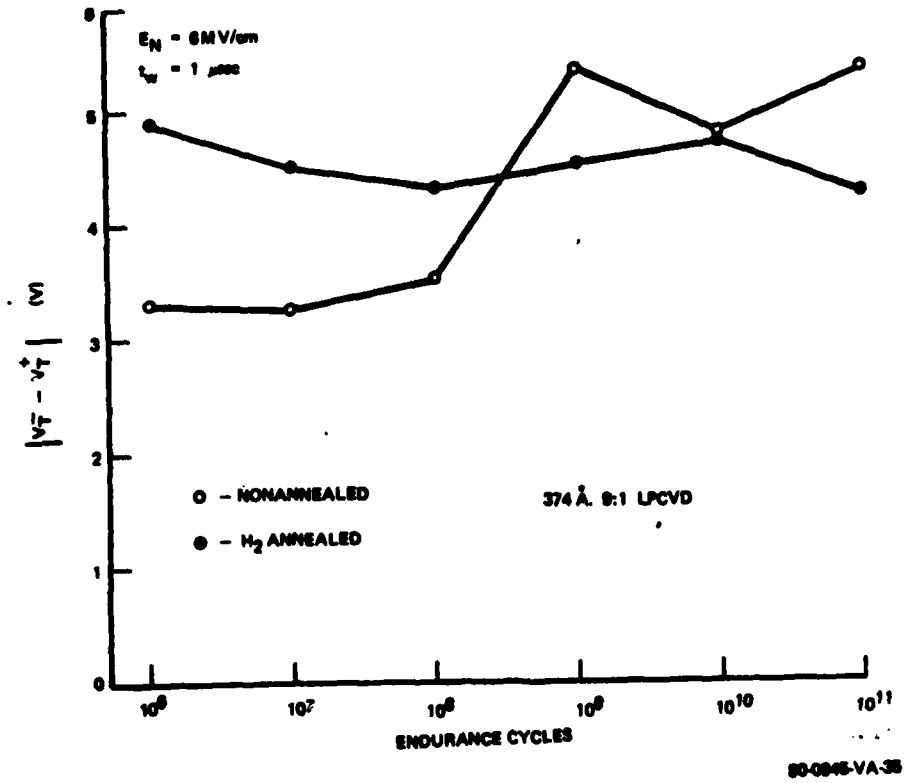


Figure 4-22 ±20V DC window vs. endurance cycles, for devices H_2 annealed and non-annealed structures. Pulse width, t_w = 1μsec, E_n=6MV/cm

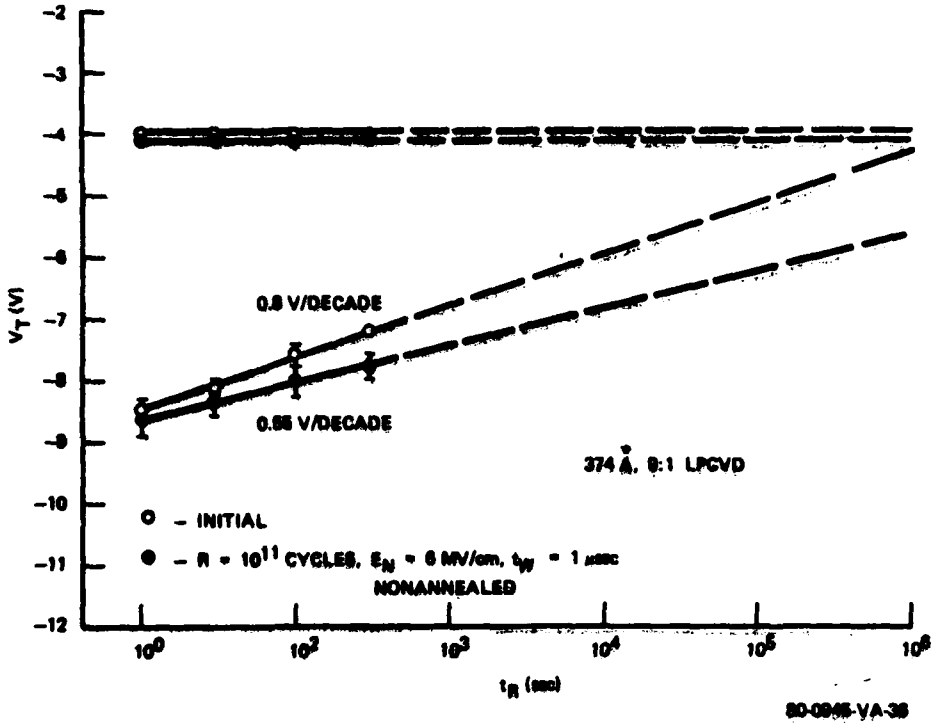


Figure 4-23. Memory window vs. time, for non-annealed device that has not been stressed and structures stressed to 10^{11} cycles. Pulse width, t_w=1μsec, E_n=6MV/cm

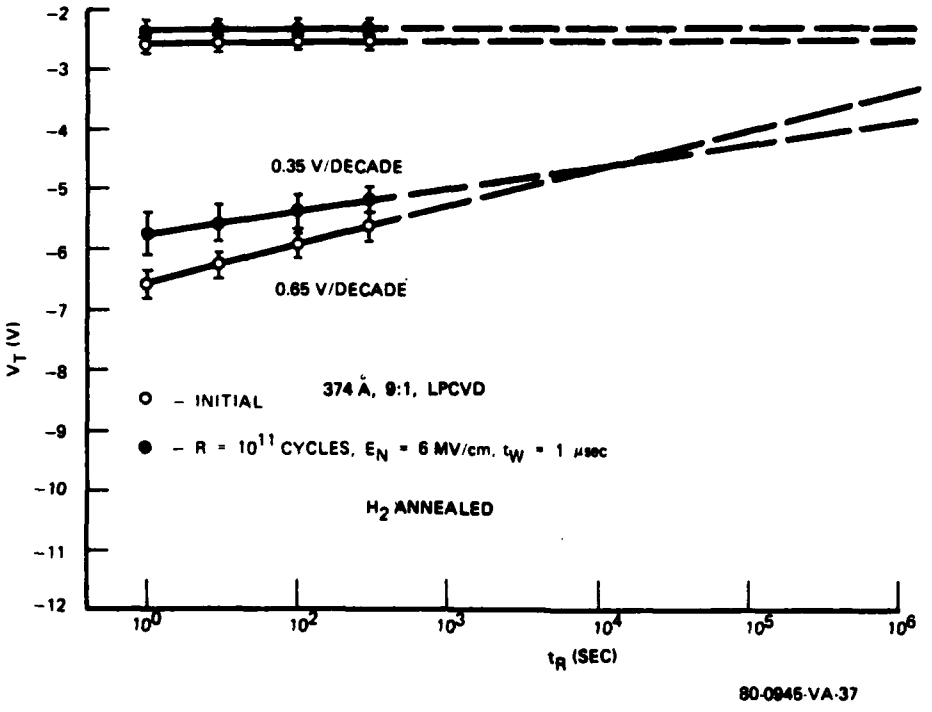


Figure 4-24. Memory window vs. time, for H_2 annealed device that has not been stressed and structures stressed to 10^{11} cycles. Pulse width t_w=1μsec E_n=6MV/cm

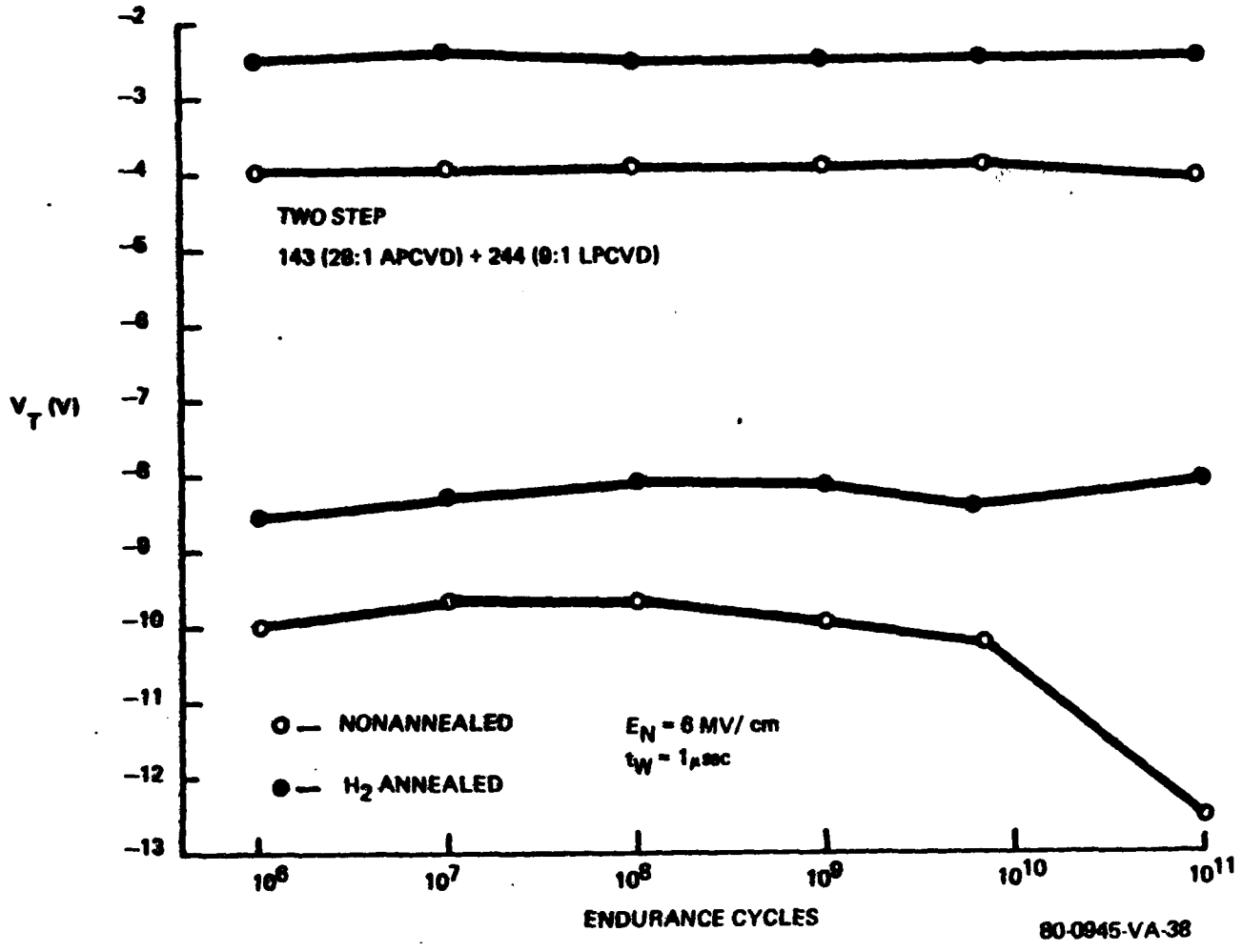


Figure 4-25. ±27V DC memory window vs. endurance cycles, for H_2 annealed and non-annealed two step nitride structures Pulse width, t_w = 1μsec E_n= 6MV/cm

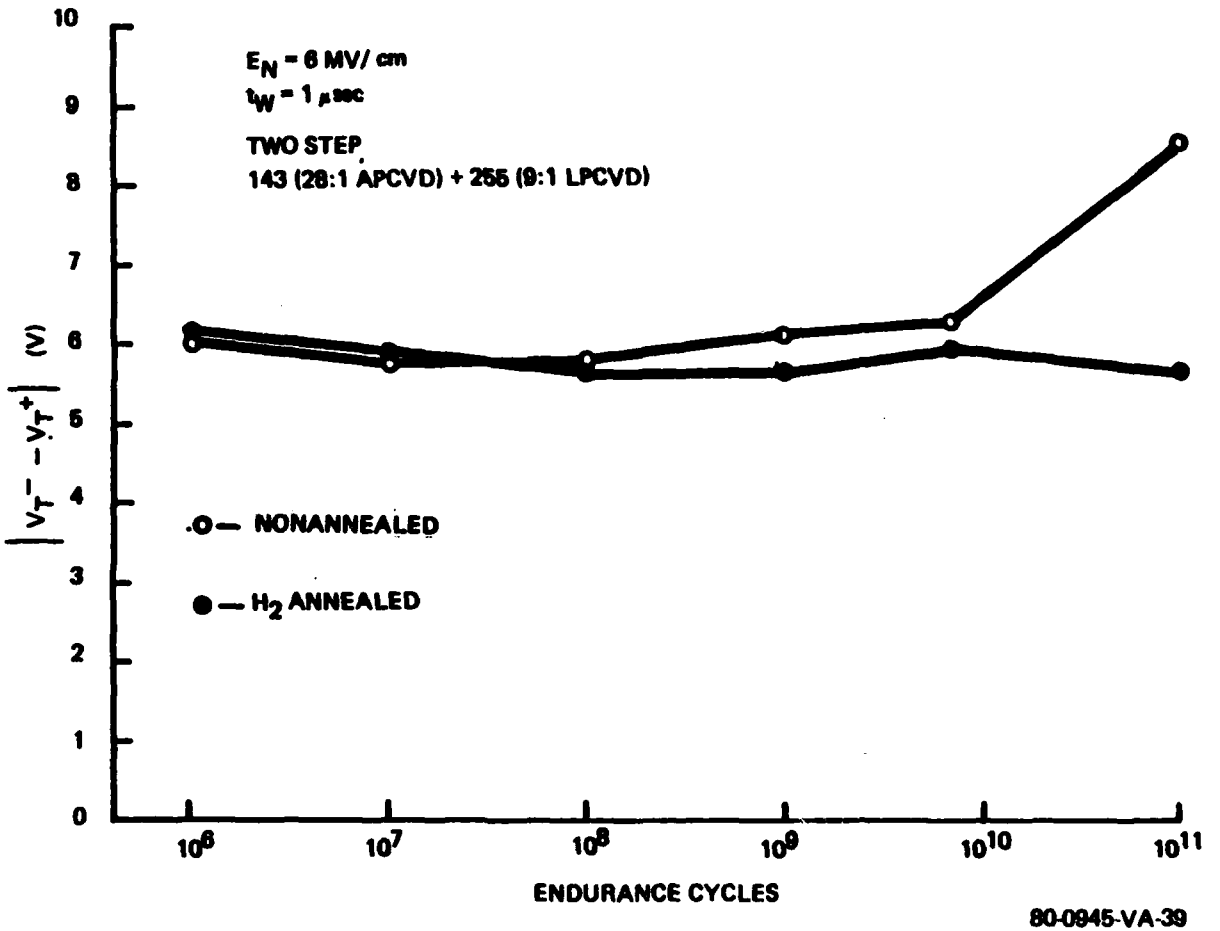


Figure 4-26. ±20V DC memory window size vs. endurance cycles, for H_2 annealed and non-annealed two step nitride structures Pulse width, t_w = 1μsec E_n= 6MV/cm

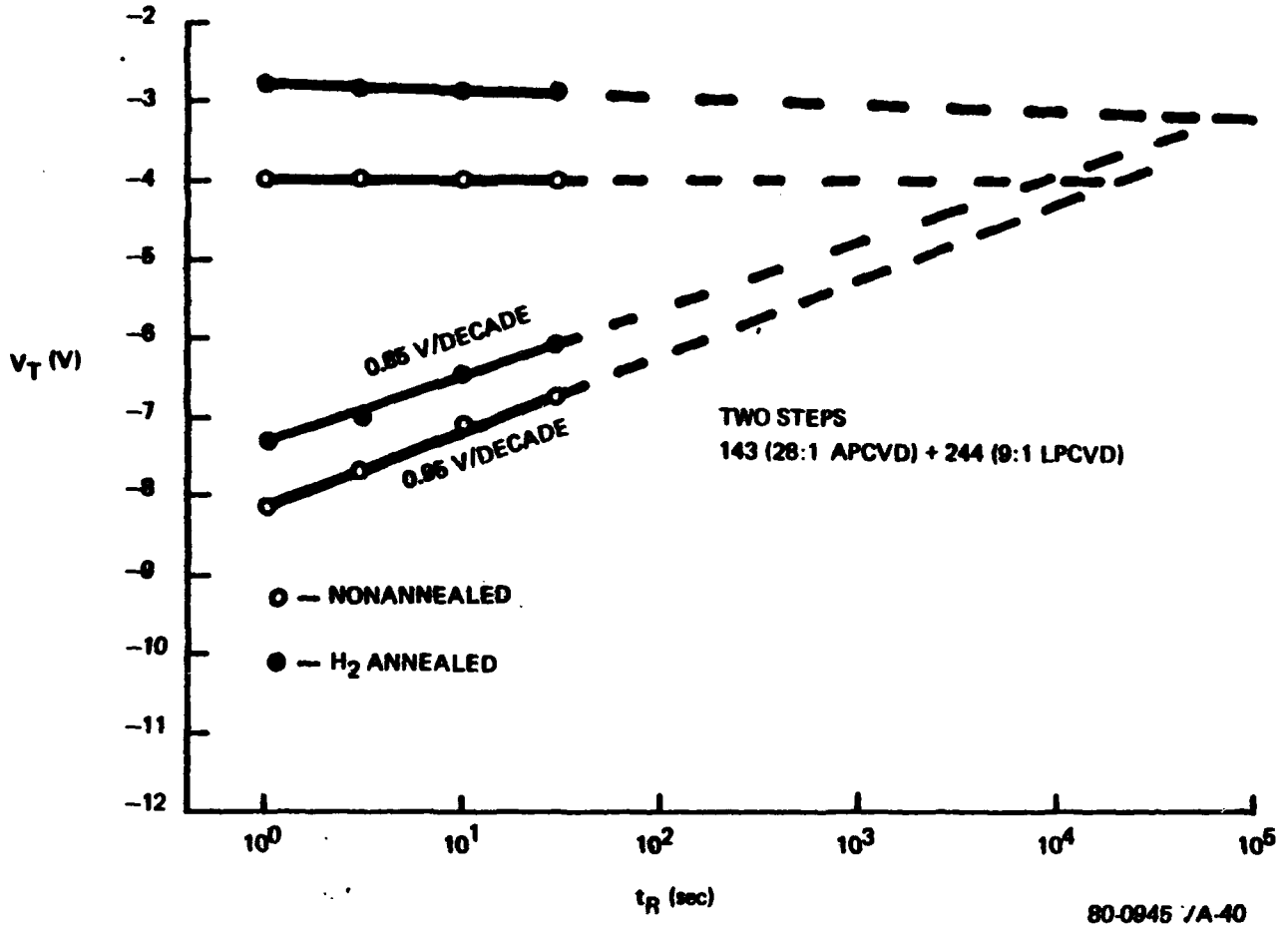


Figure 4-27. Memory window vs. time, for H_2 annealed and non-annealed two step nitride structures before endurance stressing

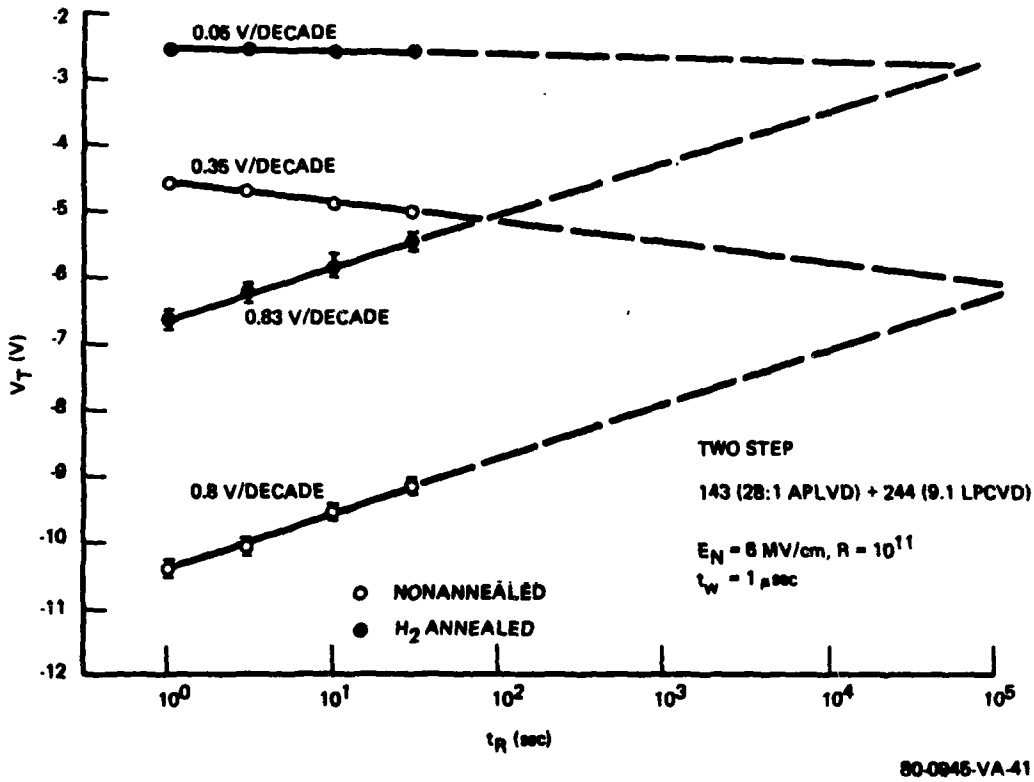


Figure 4-28. Memory window vs. time, for H_2 annealed and non-annealed two step nitride structures after 10^{11} endurance cycles. Pulse width, t_w=1μsec, E_n=6MV/cm

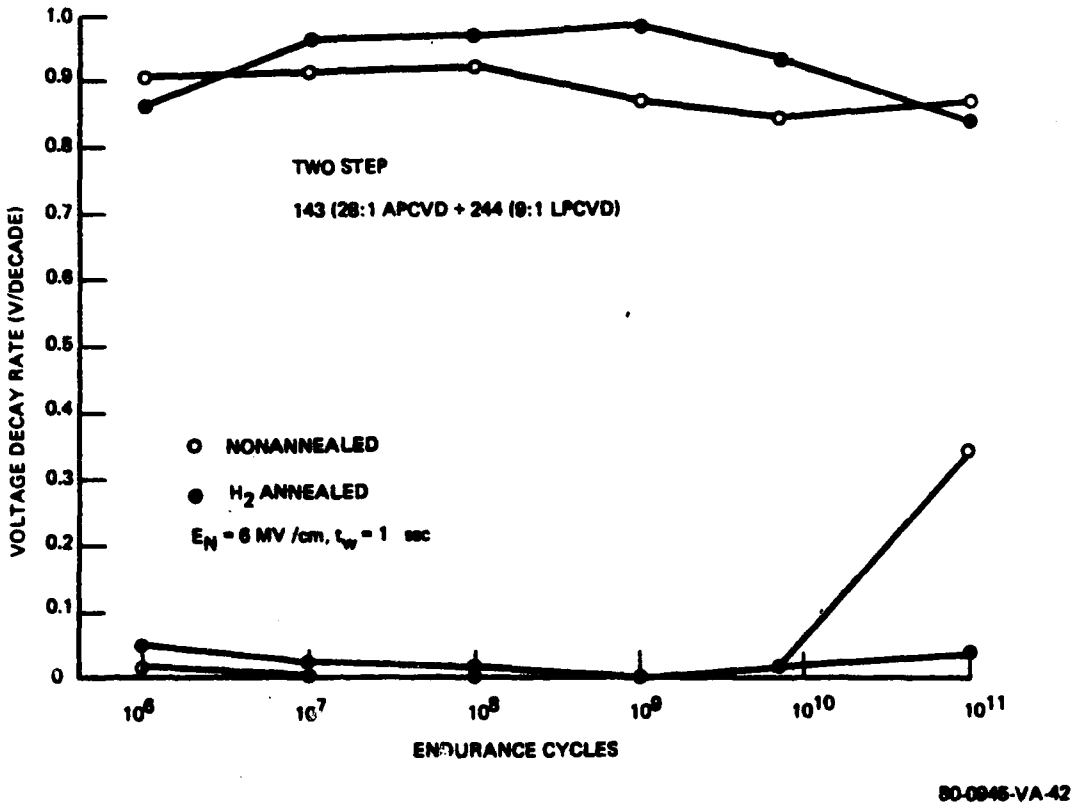


Figure 4-29. Decay rate vs endurance cycles, for H_2 annealed and non-annealed two step nitride structures. Pulse width t_w=1μsec, E_n = 6MV/cm

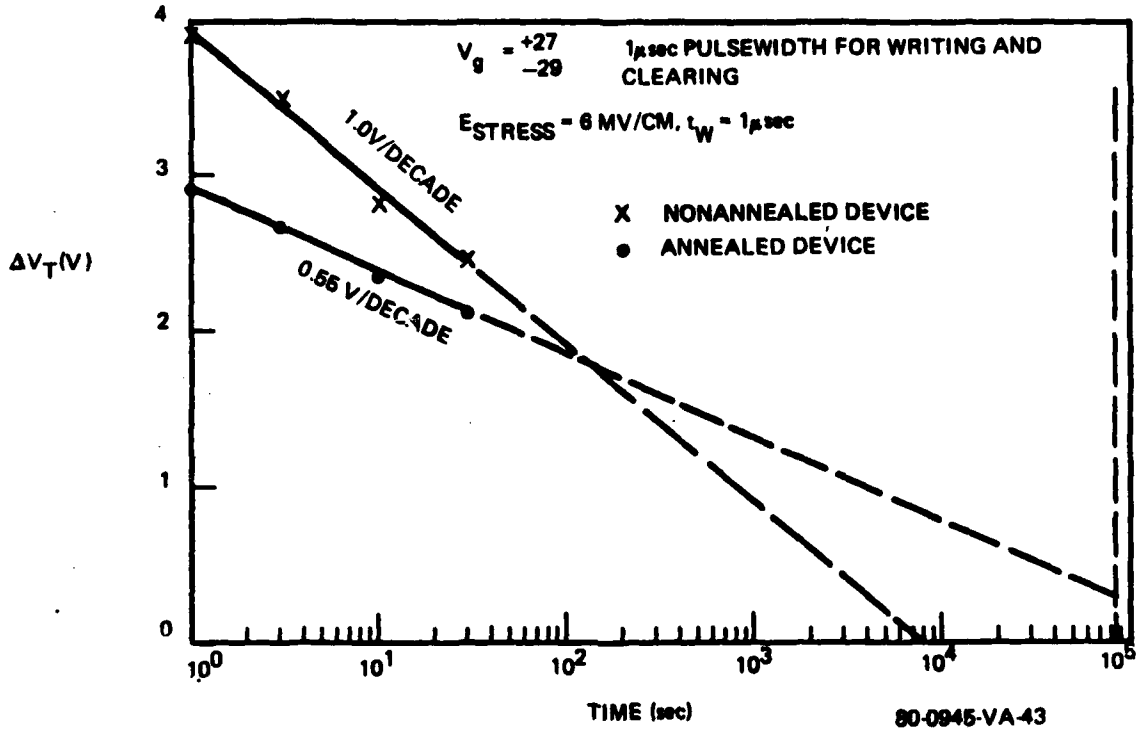


Figure 4-30. Memory window size vs. time, for H_2 annealed and non-annealed single nitride LPCVD structures. Pulse width, t_w =1μsec, E_n=6MV/cm

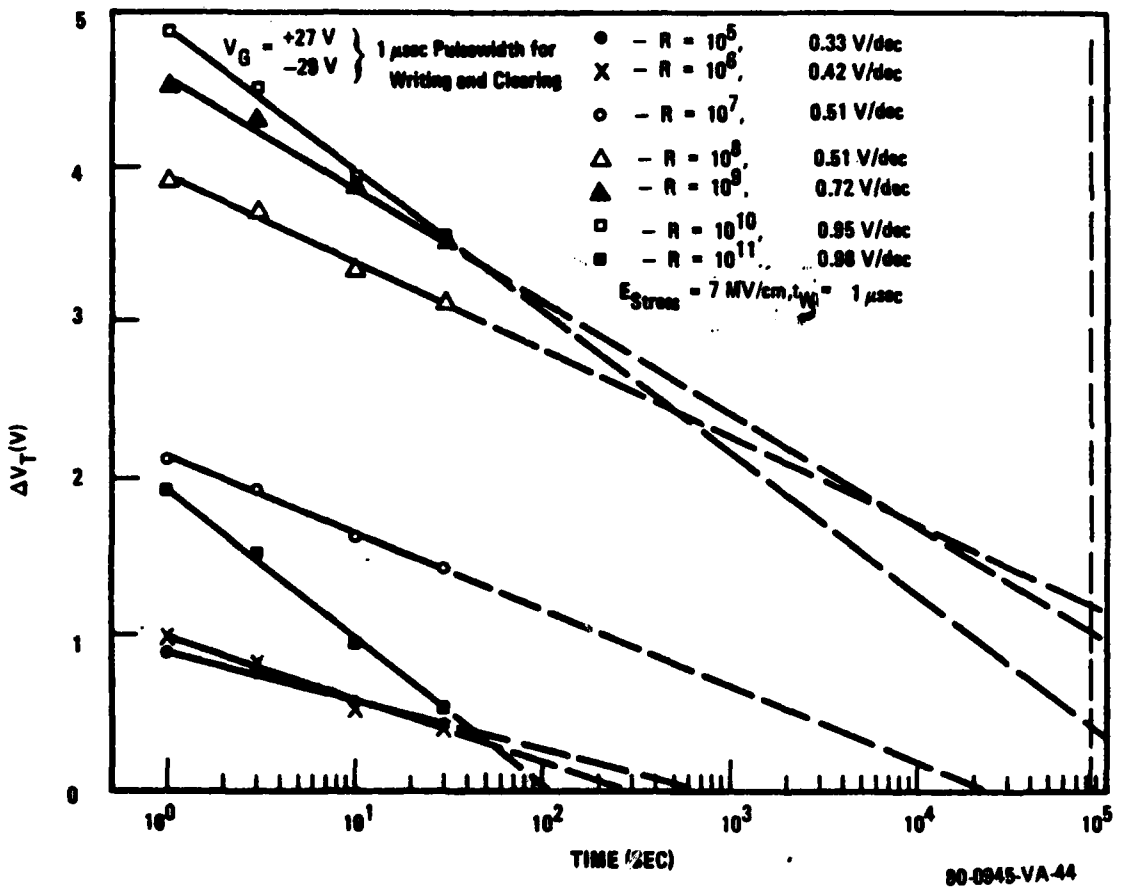


Figure 4-31. Memory window size vs. time (non-annealed devices). Pulse width, t_w=1μsec, E_n=7MV/cm

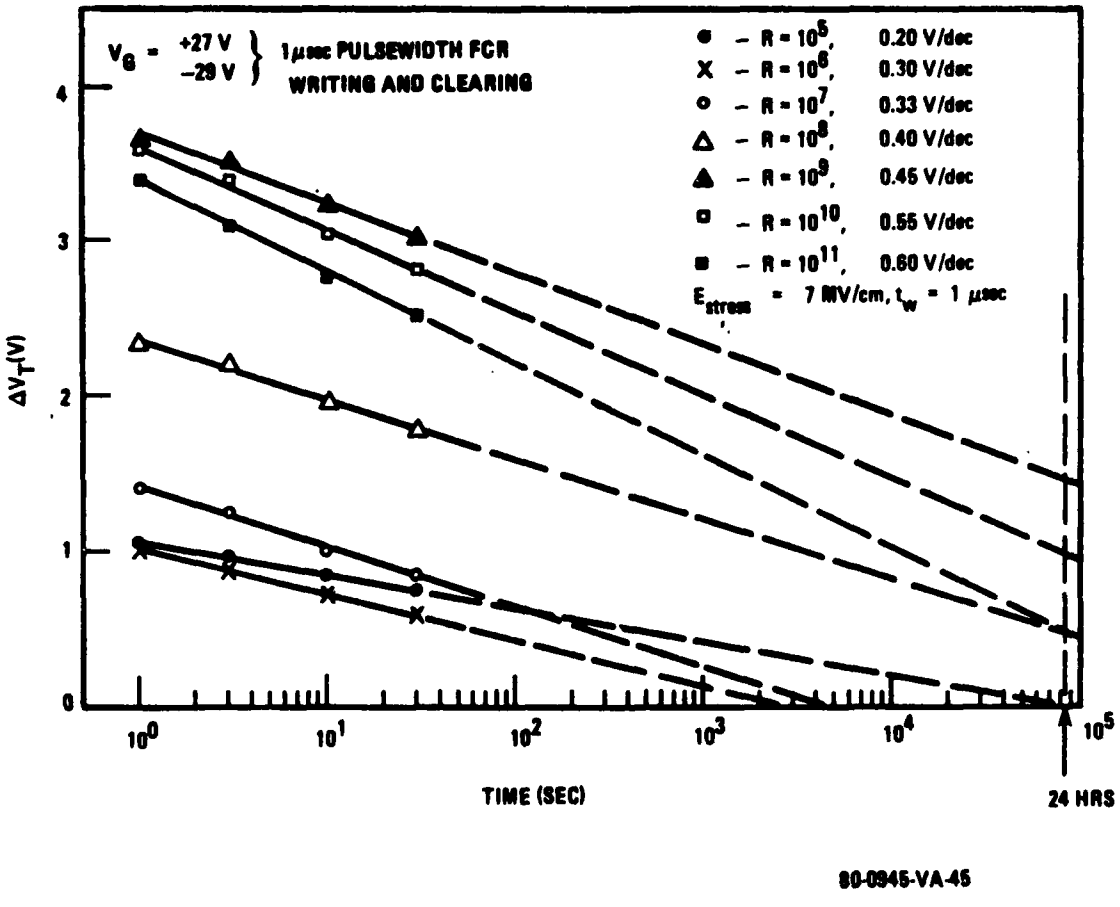


Figure 4-32. Memory window size vs. time (H_2 annealed devices). Pulse width, t_w=1μsec, E_n=7MV/cm

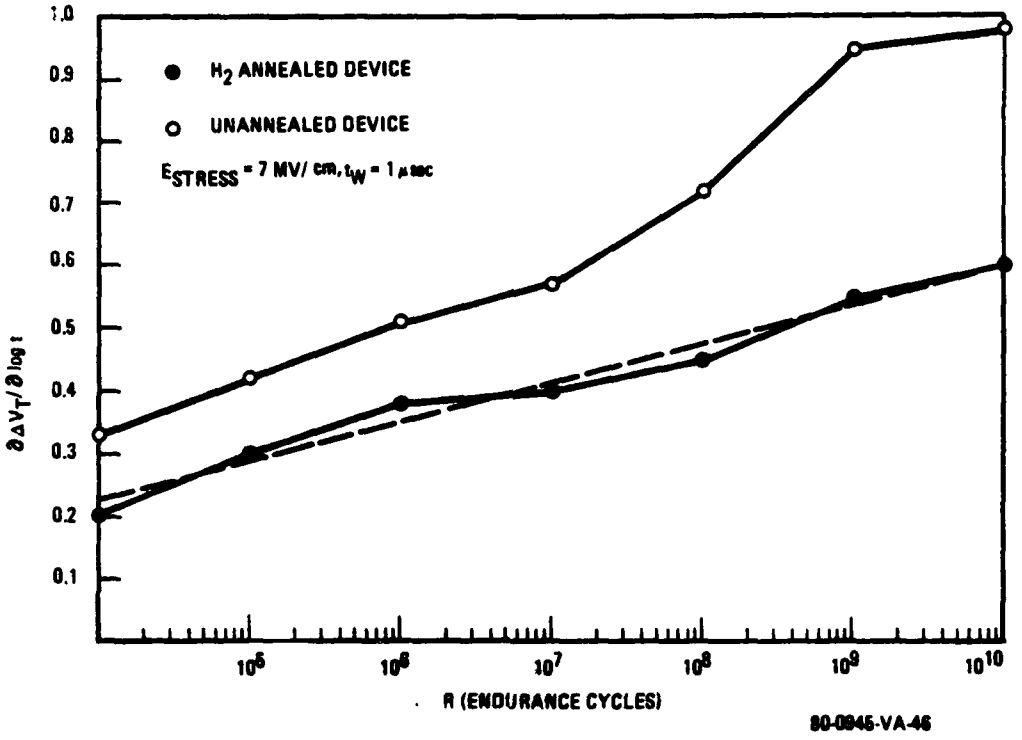


Figure 4-33. Memory decay rate vs. endurance cycles, for H_2 annealed and non-annealed devices. Pulse width, t_w=1μsec, E_n=7MV/cm

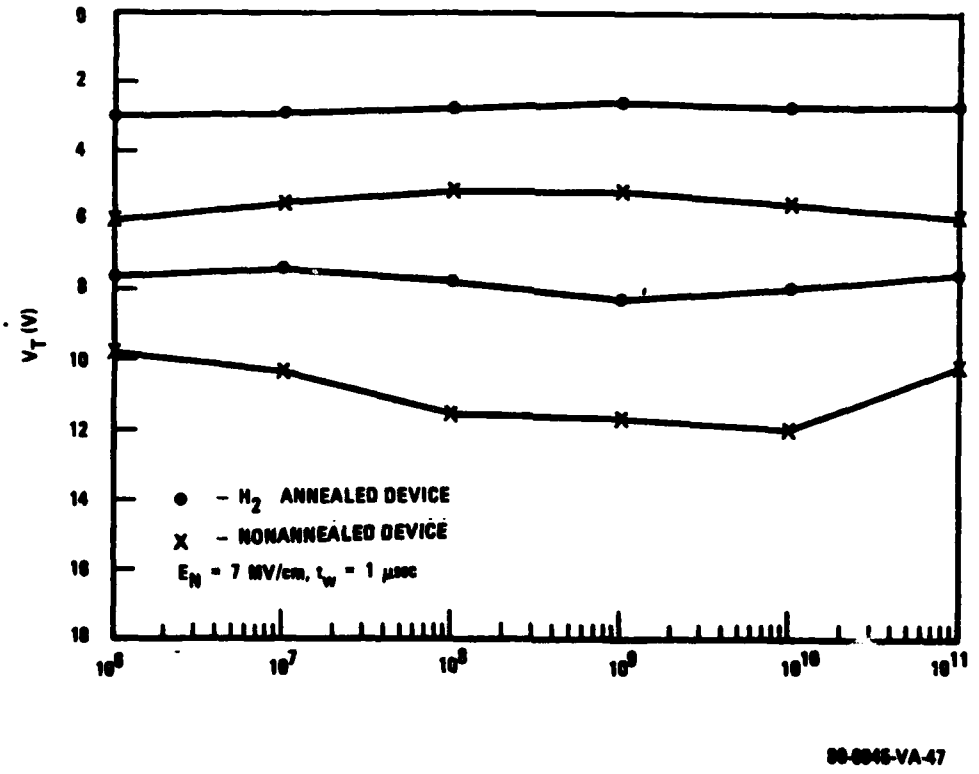


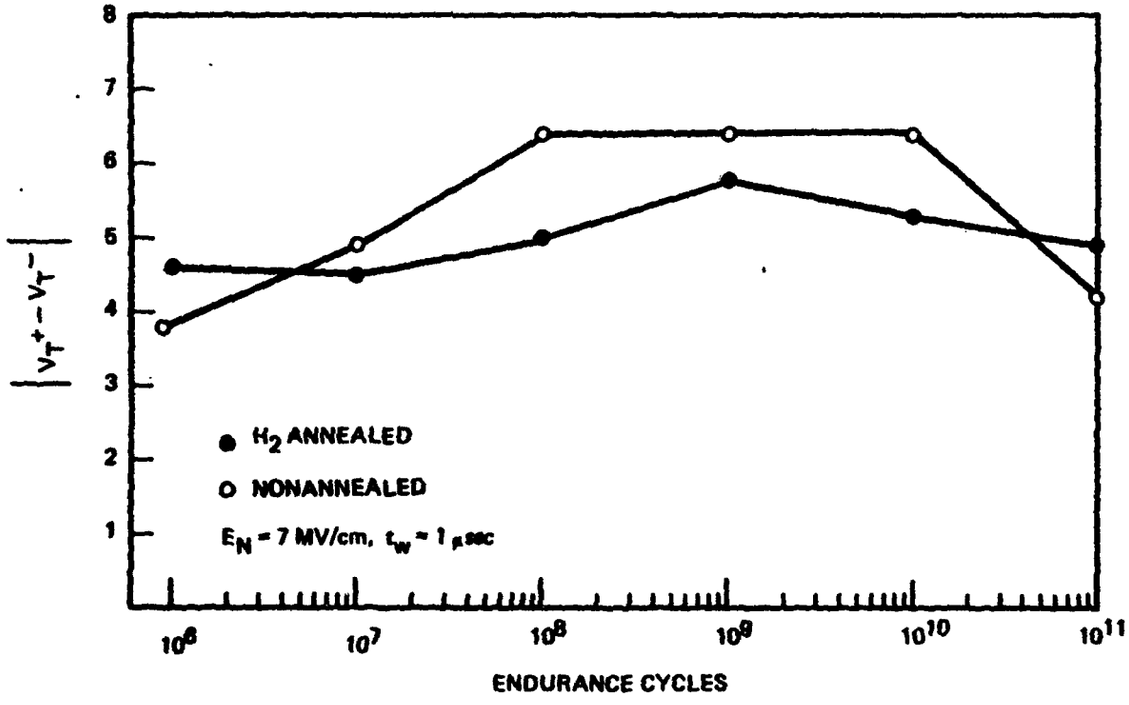
Figure 4-34. ±20V DC memory threshold voltage vs endurance cycles for H_2 annealed and non-annealed structures. Pulse width t_w=1μsec, E_n=7MV/cm

structures that were both non-annealed and H_2 annealed. The stress conditions were nitride fields of 7 MV/cm with a pulse width of lusec. The pulsed memory window sizes and decay rates were obtained with a +27 and a -29 lusec pulse width for writing and clearing. Figures 4-31 and 4-32 gives the pulsed memory window size and memory decay rate for the non-annealed devices and H_2 annealed structures respectively. The memory window size is shown as a function of time in Figure 4-33. The curves in Figure 4-34 and 4-35 depicts the $\pm$20V DC memory threshold voltage levels and memory window size respectively as a function of endurance cycles.

4.6 γ Total Dose Radiation Results

The effect total dose radiation has on various device types and gate dielectric structures have been investigated. The testing was performed using the Co^{60} source at Hanscom AFB, Ma. Data were collected at total dose intervals of 10K, 50K, 100K, 500K and 1M Rad. A dose rate of 42K rads/min was used. The devices were measured immediately after irradiation to reduce short term annealing. The maximum time between the end of one dose level and the beginning of another dose level was about 45 min. The measurement included sweeping out the C-V curve in the case for capacitors and measuring threshold voltages when transistors were being tested.

The total dose raidation hardness of the following



80-0945-VA-48

Figure 4-35. ±20V DC memory window vs. endurance, for H_2 annealed and non-annealed structures. Pulse width, t_w=1μsec, E_n=7MV/cm

device types has been evaluated:

(1) An all oxide polysilicon gate capacitor structure fabricated in an n-type bulk silicon substrate oriented in the <100> direction. A Segment of a MNOS/CMOS process was used to process the capacitors.

(2) P-channel transistors with a dual dielectric (SiO_2 / Si_3N_4) gate structure fabricated in Silicon On Sapphire (SOS) using a MNOS/SOS process.

(3) N-channel transistor with an all oxide polysilicon gate structure. The devices were fabricated using a MNOS/CMOS process. The starting material consisted of a n-type substrate oriented in the <100> direction.

(4) Un-protected p-channel polysilicon gate MNOS memory transistors. The devices were fabricated with a MNOS/CMOS process.

4.6.1 All oxide polysilicon gate capacitor structures.

The devices were fabricated with a MNOS/CMOS

process. The starting material was an N <100> bulk silicon substrate, with a resistivity of 3-9 Ω-cm. The gate oxide was grown at 900°C to 830A using a dry wet dry process. 6KA of polysilicon was then deposited and subsequently phosphorus doped. The polysilicon was oxidized at 900°C followed by a 490A LPCVD silicon nitride deposition. The process sequence of the gate structure is summmarized in Table 4-10. An initial charge associated with the SiO_2 structure was calculated to be $2.2X10^{11}/cm^2$.

The Capacitance-Voltage (C-V) plots in Figure 4-36 and 4-37 shows temperature bias stress stabilty results for these structures. Each curve represents a different wafer, with a sample size of 5 taken from each wafer. The devices were stressed to a voltage level of ±20V at a temperature of 185°C. The stress cycle was conducted as follows. The pre-stressed curve was obtained at room temperature. The device was then subjected to a +20V bias and the temperature was increased to 185°C. This temperature was held for 5 minutes while the voltage was maintained at +20V. The structure was subsequently cooled to room temperature under the constant voltage bias. At room temperature the bias was removed and the +20V stress curve obtained by sweeping the C-V curve from a +6V to -14V. The -20V stress curve was produced by the same procedure given for the +20V polarity. The C-V curve was obtained by sweeping from a -14V to +6V.

Table 4-10. Process sequence for all oxide polysilicon gate capacitor structures.

Oxidation
- Dry - 30 min
- Wet - 25 min
- N_2 - 30 min
- 900°C
- X_{ox} - 830A

Polysilicon Deposition
- X = 6KA

Polysilicon Doping
- Phosphine Source
- 18 min
- 900°C

Polysilicon Oxidation
- Dry - 30 min
- Wet - 25 min
- N_2 - 30 min
- X_{ox} 810A

Nitride Deposition
- LPCVD
- NH_3:$SiCl_2H_2$ = 9:1
- 750°C
- X_N = 490A

81-1025-V-32

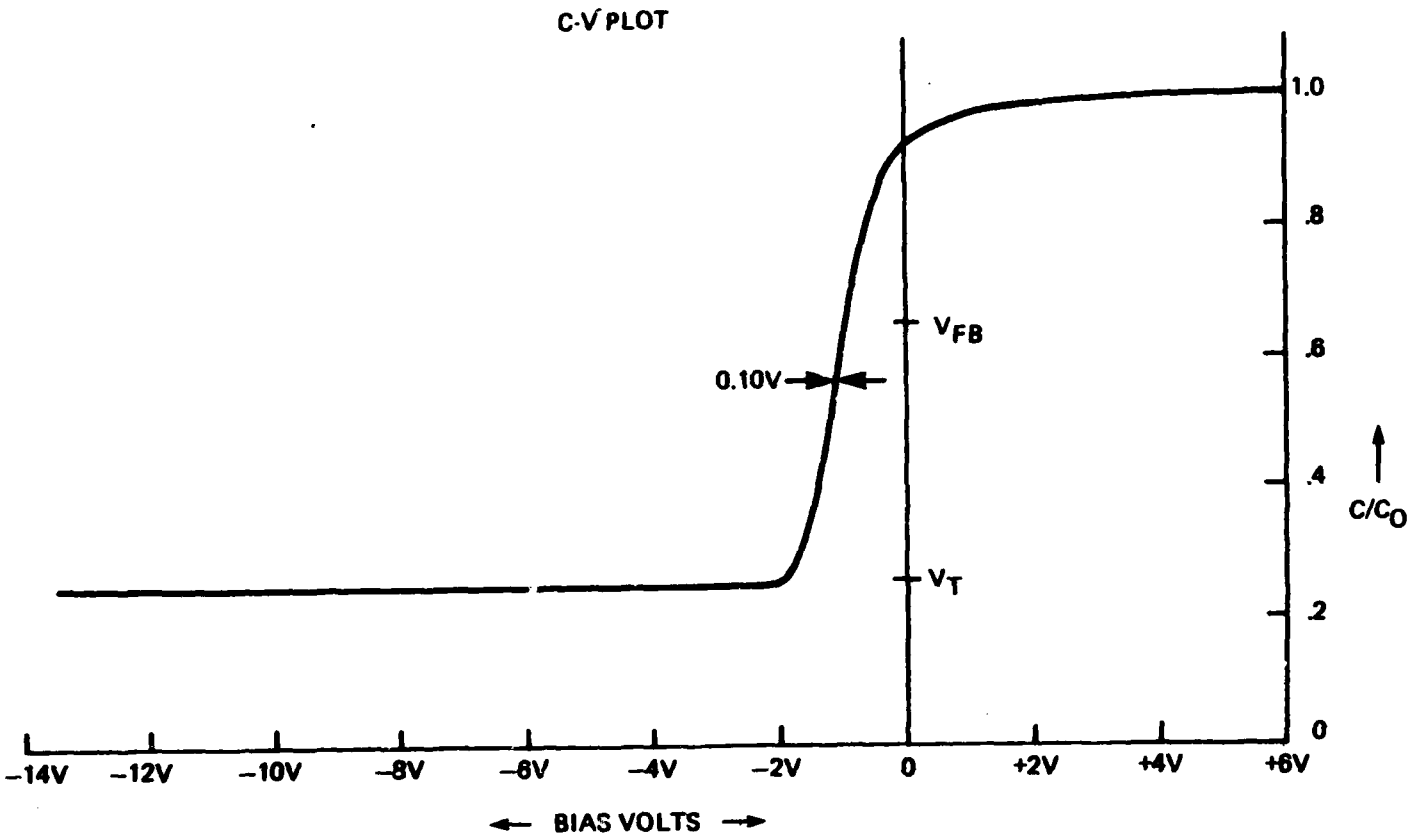


Figure 4-36. C-V plot showing ±20V, 185°C TBS stability test for all oxide polysilicon gate device structure. X_{ox}=830A, Sample size = 5, Wafer #7

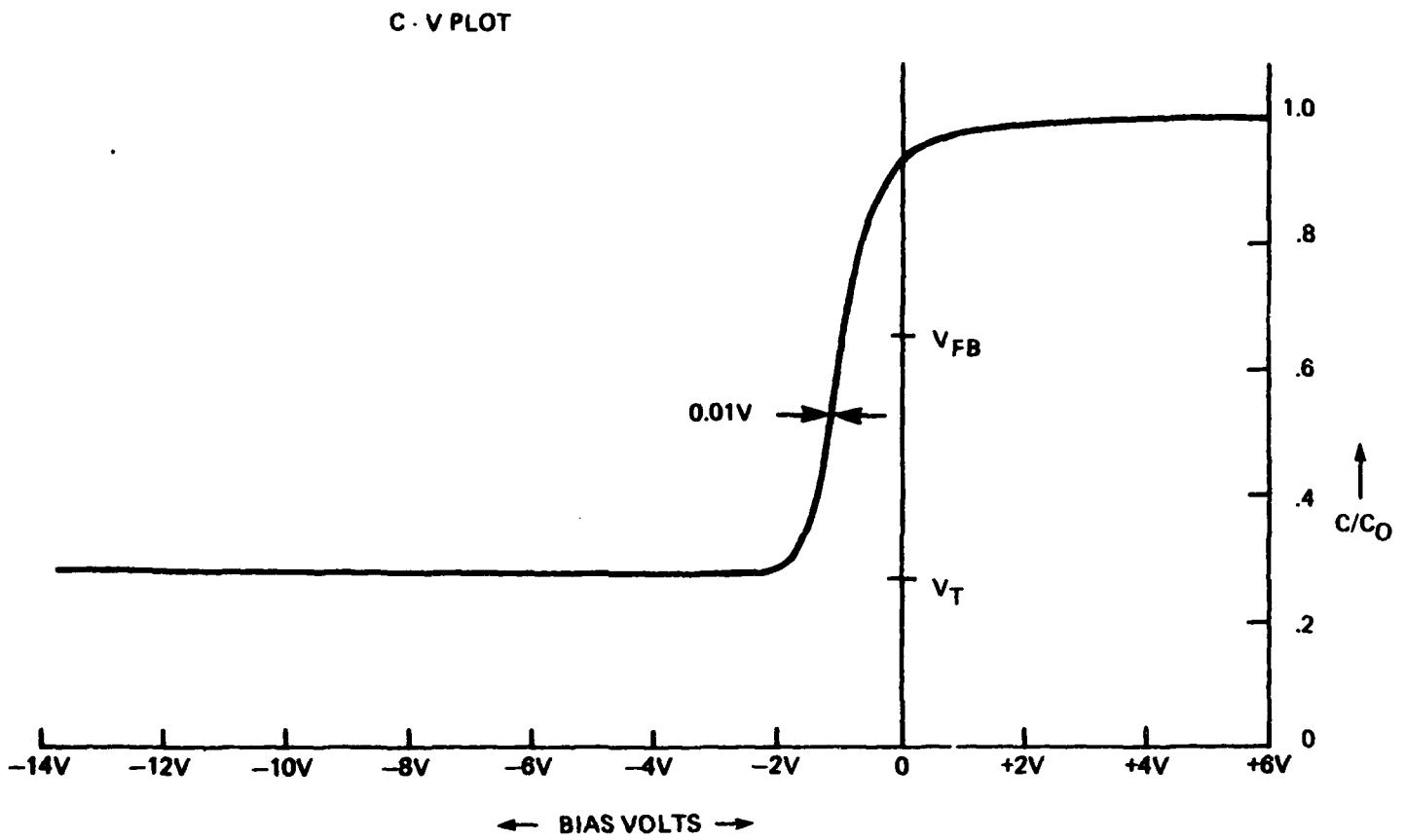


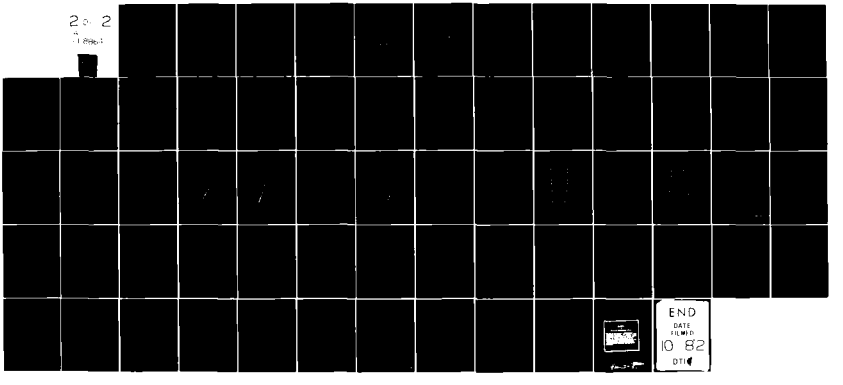
Figure 4-37. C-V plot showing ±20V, 185°C TBS stability test for all oxide polysilicon gate device strcutre. X_{ox} = 830A, sample size=5, Wafer #8

The flatband voltage shift and threshold voltage variations are plotted as a function of total dose radiation in Figures 4-38 thru 4-41. The flatband voltage was observed to be at C/C_o = 0.65. The point on the C-V curve where the device begins to go into deep inversion was taken to be the threshold voltage. The change in threshold and flatband voltage for devices that did not have a bias applied to the gate is shown by the curves in Figure 4-38. Large threshold voltage changes are observed after 100K rads(Si) while the flatband voltage change is not as pronounced. Similar trends are noted when the gate is biased with a -8V, -18V, and +12V. The change in both threshold and flatband voltage are greatest when the gate was biased with a +12 volts. Here, a threshold voltage shift of less than about 2V occur up to a total dose level of about 100K rad (Si). The curves in Fgure 4-42 gives the change in threshold voltage as a function of total dose radiation for each bias condition V_G=0V, -8V, -18V and +12V. The curves shown in Figure 4-43 depict the flatband voltage change with total dose γ radiation. From these plots it is noted that the +12V gate bias is the most severe condition the strucures are subjected to.

4.6.2 Dual dielectric MNOS/SOS Transistor Structures

The Metal Nitride Oxide/Silicon On Sapphire

AD-A118 864 WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER B--ETC F/G 9/5
MNOS/SOS RADIATION HARDNESS PERFORMANCE AND RELIABILITY STUDY.(U)
MAY 82 F L HAMPTON, J R CRICCHI F19628-79-C-0133
UNCLASSIFIED RADC-TR-82-89 NL



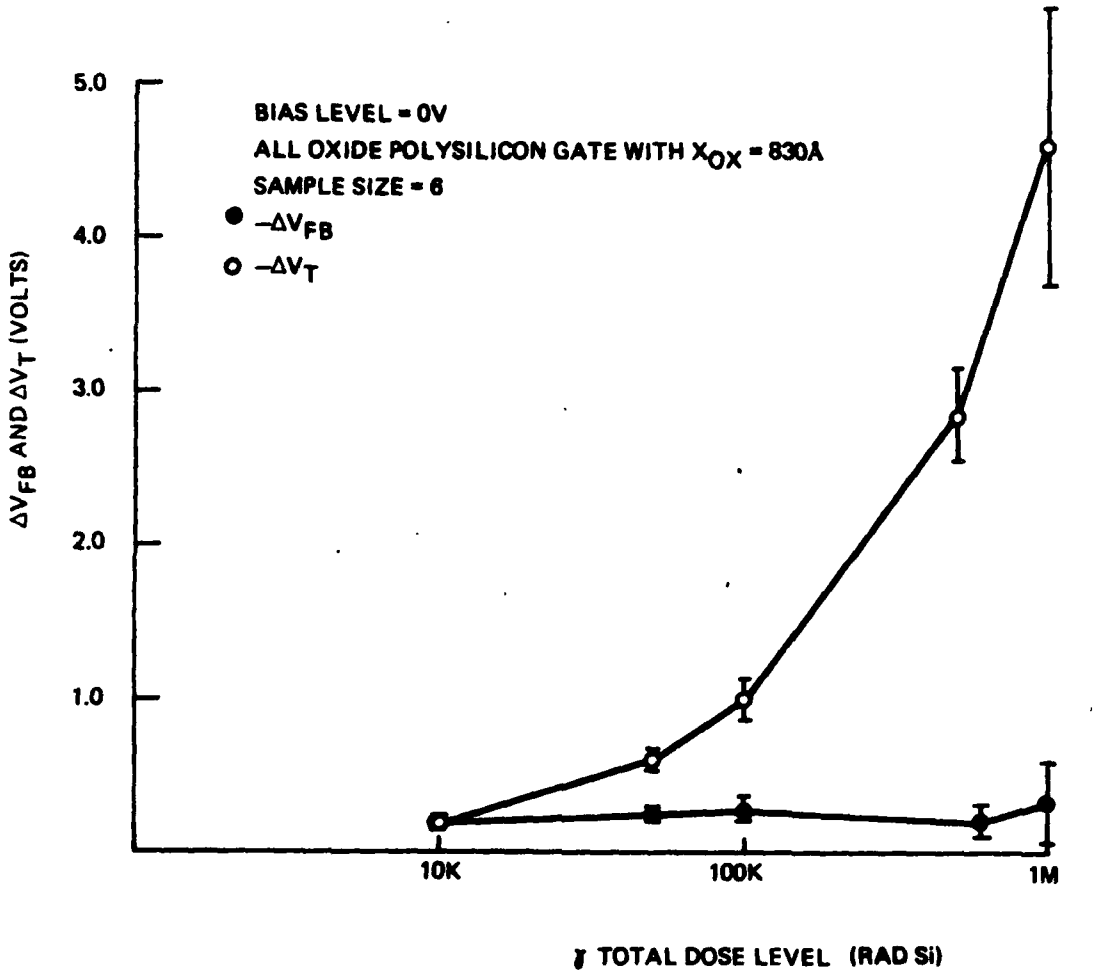


Figure 4-38. Change in flatband and threshold voltage as a function of total dose γ radiation. All oxide polysilicon gate capacitor structures, V_G=0V.

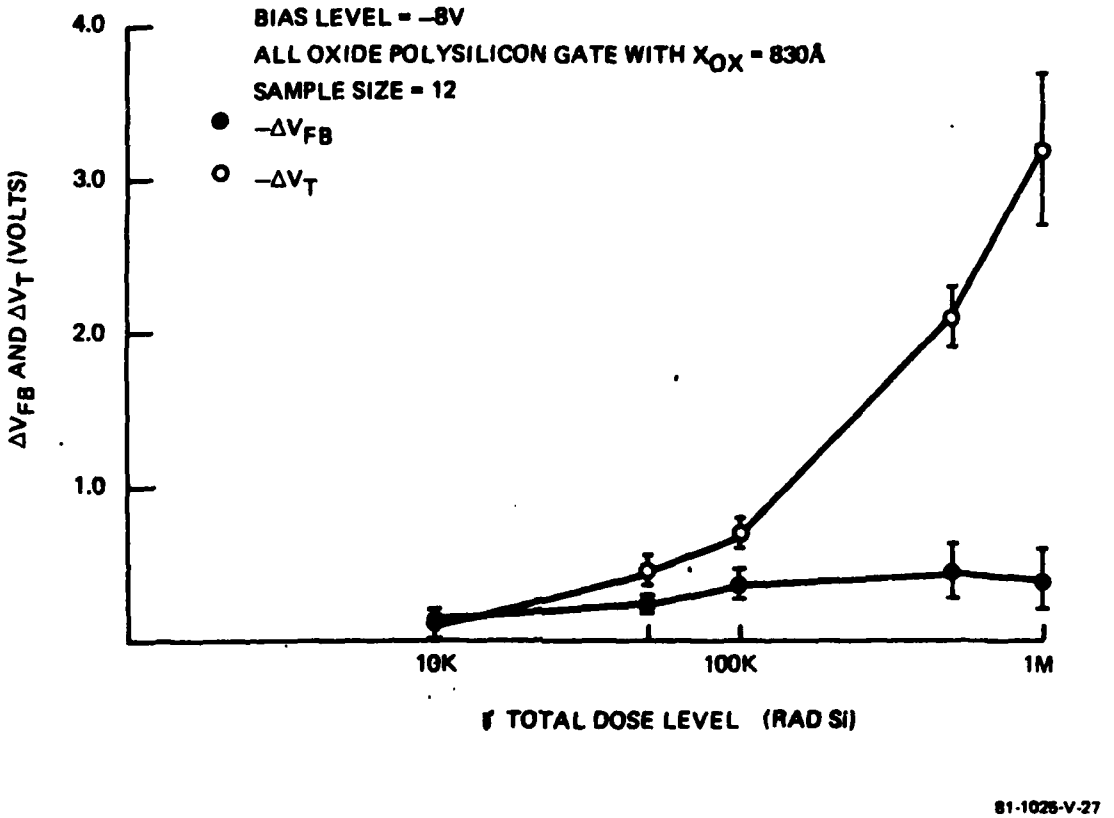


Figure 4-39. Charge in flatband and threshold voltage as a function of total dose γ radiation. All oxide polysilicon gate capacitor structure. V_G=-8V

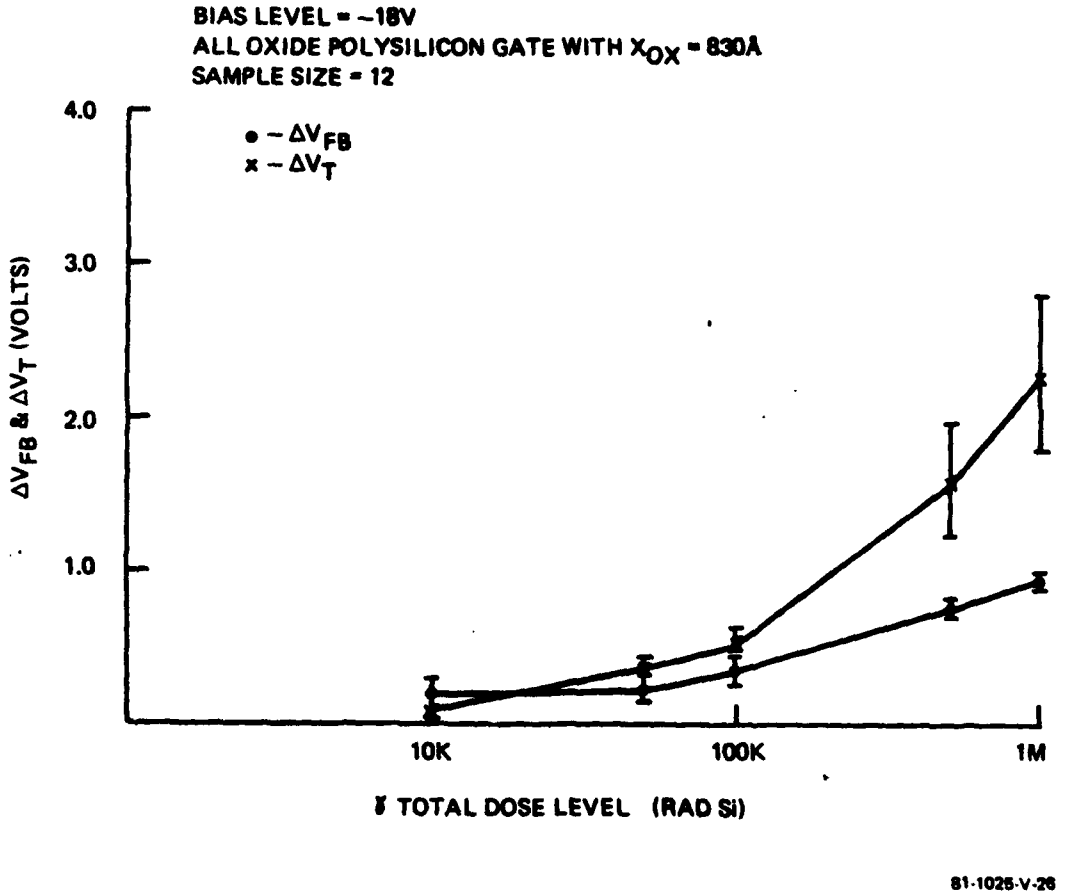


Figure 4-40. Change in flatband and threshold voltage. As a function of total dose γ radiation. All oxide polysilicon gate capacitor structures. V_G=-18V.

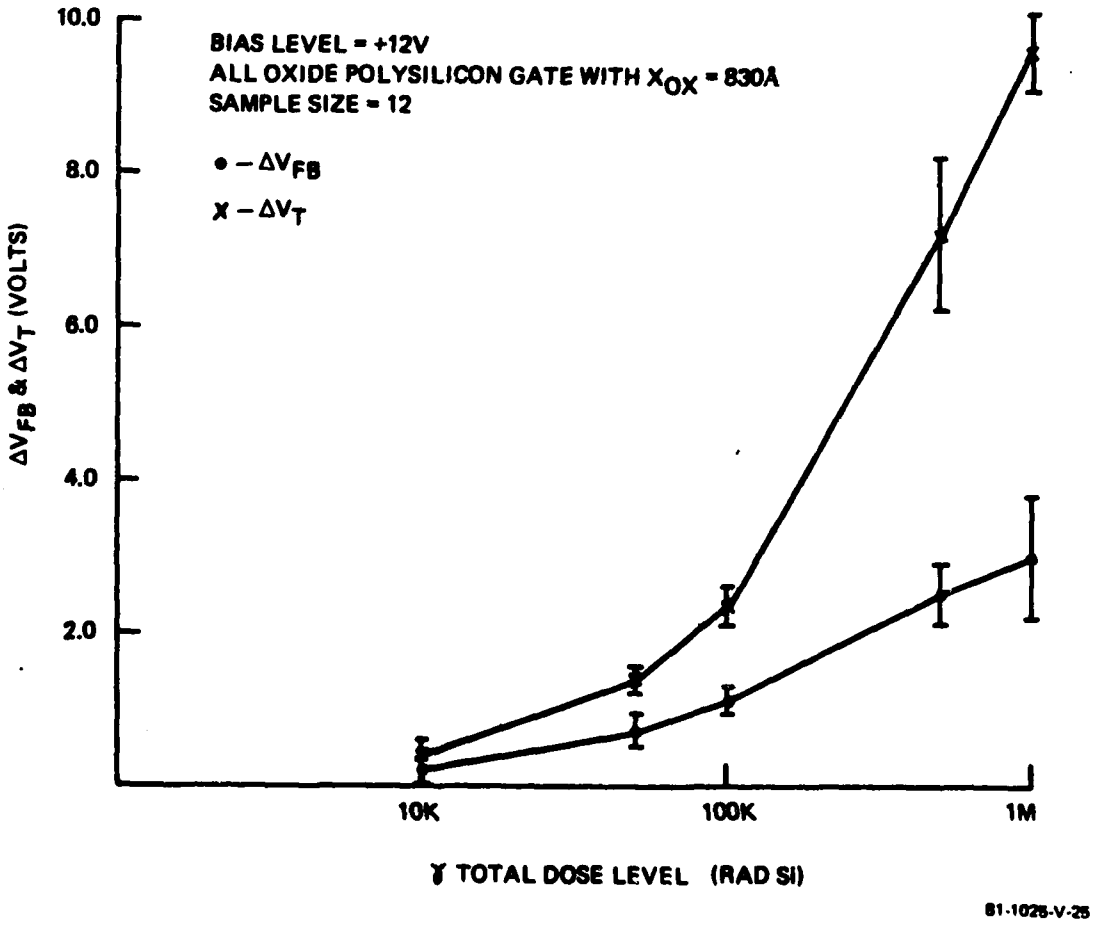


Figure 4-41. Change in flatband and threshold voltage as a function of total dose γ radiation. All oxide poly-silicon gate capacitor structures. V_G=+12V.

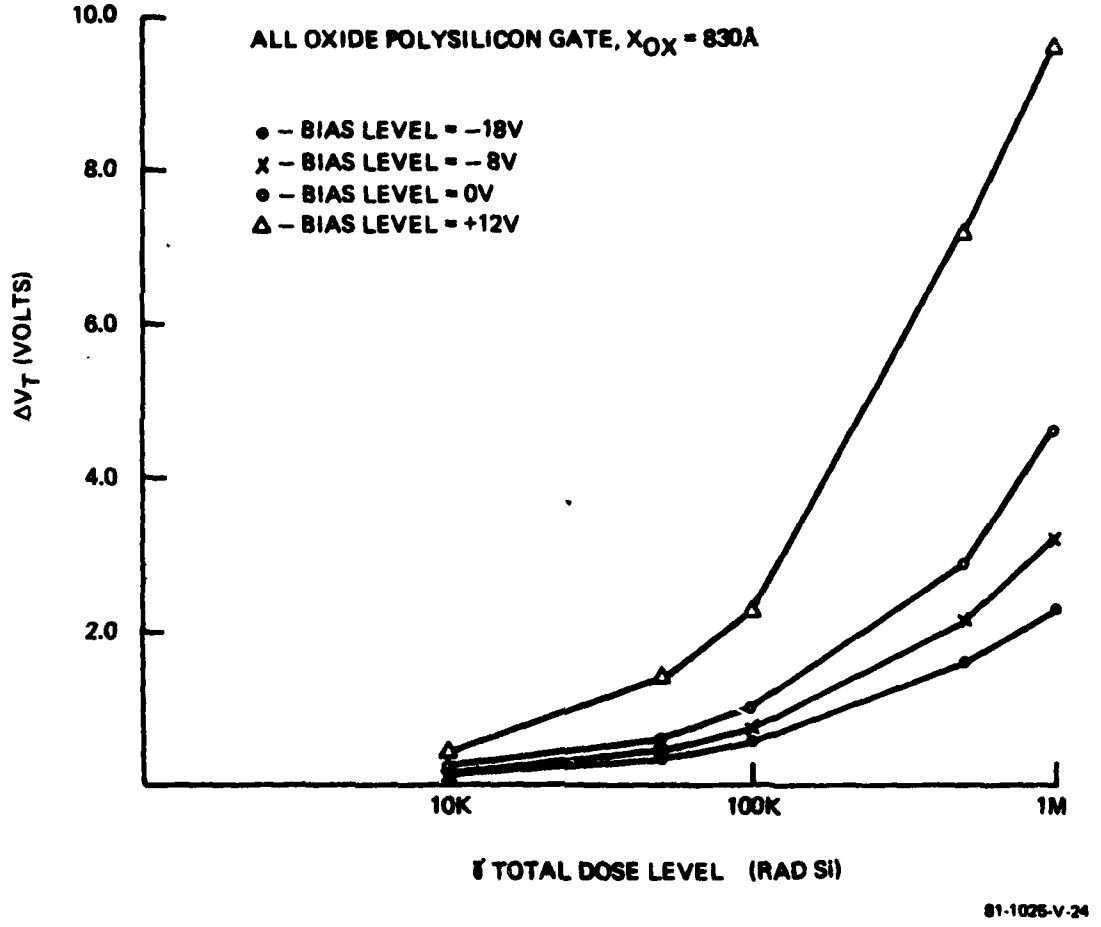


Figure 4-42. Variations in threshold voltage change with total dose γ radiation from various gate bias levels. All oxide polysilicon gate capacitor.

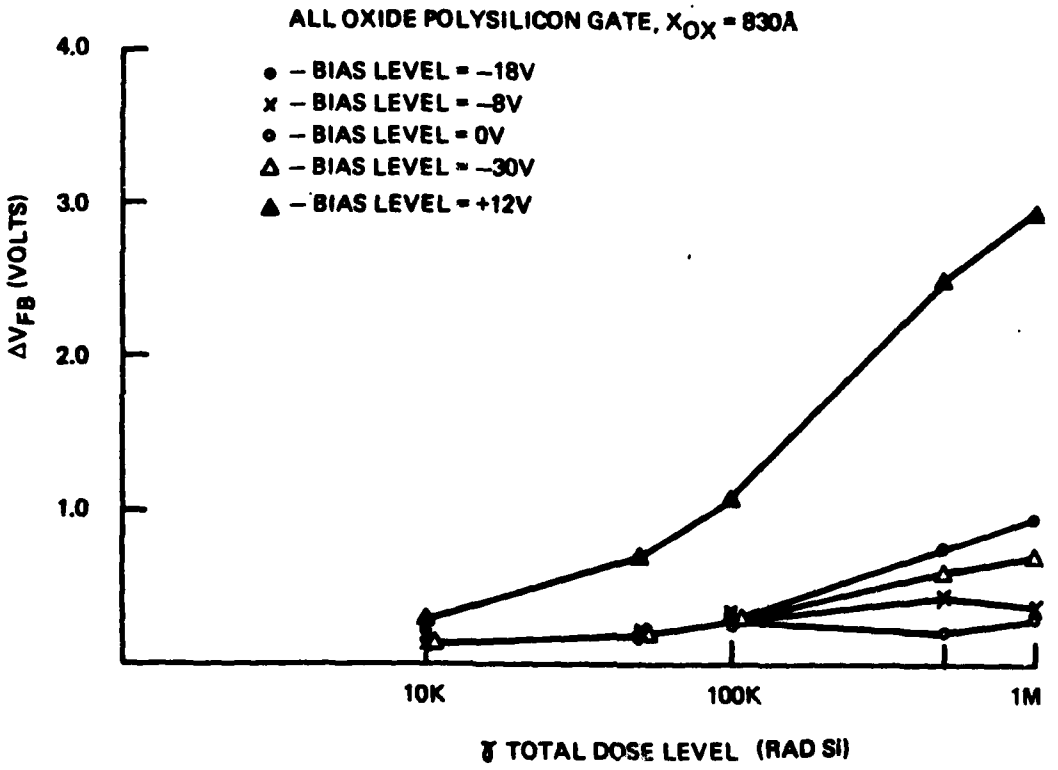


Figure 4-43. Variation in flatband voltage change with total dose γ radiation for various gate bias levels. All oxide polysilicon gate capacitors.

(MNOS/SOS) process was used to fabricate the dual dielectric (SiO_2/Si_3N_4) gate structures. An oxide thickness of 77A was grown followed by a 1457A silicon nitride deposition. The nitride was deposited with a low pressure chemical vapor deposition reactor. The film was deposited with an ammonia (NH_3) to dichlorosilane ($SiCl_2H_2$) ratio of 9:1 at a temperature of 750°C, see Table 4-11. Note that the nitride layer consist of two depositions, a thick film (1083A) followed by the memory nitride (374A). Some of the devices had an oxidation and followed by an H_2 anneal incorporated into the process immediately following the memory nitride deposition. The transistors evaluated were p-type. The following gives the five (5) dfferent biasing levels and associated channel lengths that were used:

(1) Transistor T1; V_{GS} =-12V, V_{DS} = 0V, L=4um

(2) Transistor T2; V_{GS} =0V, V_{DS} = -20V, L=4um

(3) Transistor T3; V_{GS} =-30V, V_{DS}=0V, L=7um

(4) Transistor T4; V_{GS} =-20V, V_{DS} =0V, L=7um

(5) Transistor T5; V_{GS} =0V, V_{DS} =-30V, L=9um

V_{GS}, is the gate to source voltage, V_{DS}, the drain to

Table 4-11. Process sequence for dual dielectric device structures

Oxidation

Dry O_2, 11 min
900°C
X_{ox} = 77A

Fixed Threshold Nitride

LPCVD
750°C
NH_3:$SiCl_2H_2$ = 9:1
X_N = 1083Å

Memory Nitride

LPCVD
750°C
NH_3:$SiCl_2H_2$ = 9:1
X_N = 374Å

Anneal

100% H_2
900°C
30 Minutes

81-1025-V-33

source voltage, and L, the channel length of the device. The diagrams in Figure 4-44 present the circuit configuration and biasing schemes used to establish the above conditions.

The variation in threshold voltage is shown as a function of total dose radiations in Figure 4-45 thru 4-52. The threshold voltage was taken to be the gate voltage necessary to produce a drain to source current (I_{DS}) of 10uA with a drain to source voltage (V_{DS}) of -10V. The curves in Figure 4-45, show the threshold voltage as a function of total dose radiation for structures that were annealed in H_2 and those that did not have an anneal. The biasing condition of T1 was used in this case. It is noted that both curves are similar in behavior. An increasing negative shift in the threshold voltage occurs as the total dose level increases. In Figure 4-46 it is seen that the threshold voltage of the structure that was annealed in H_2 and biased using the configuration T2, tends to shift negative as the total radiation dose increased. The threshold voltage of the devices that were not annealed shifted in a positive direction relative to the initial threshold voltage value of the structures prior to being irradiated. The same behavior was observed for the devices that were biased under the condition of T5. The difference in biasing condition between T2 and T5 is the voltage applied between the drain and source, see Figure 4-44. T2 has -20V applied between drain and source, while a drain-source bias of T5 was -30V. Thus a -10V difference

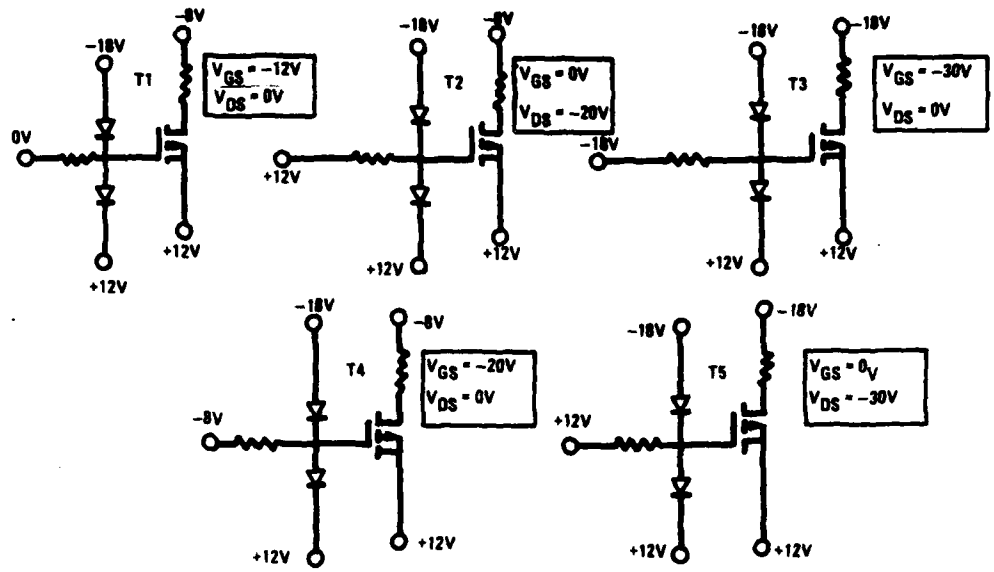


Figure 4-44. Circuit configuration and biasing scheme for radiation testing. Transistor structures consist of SiO_2/Si_3N_4 gate fabricated using a MNOS/SOS process.

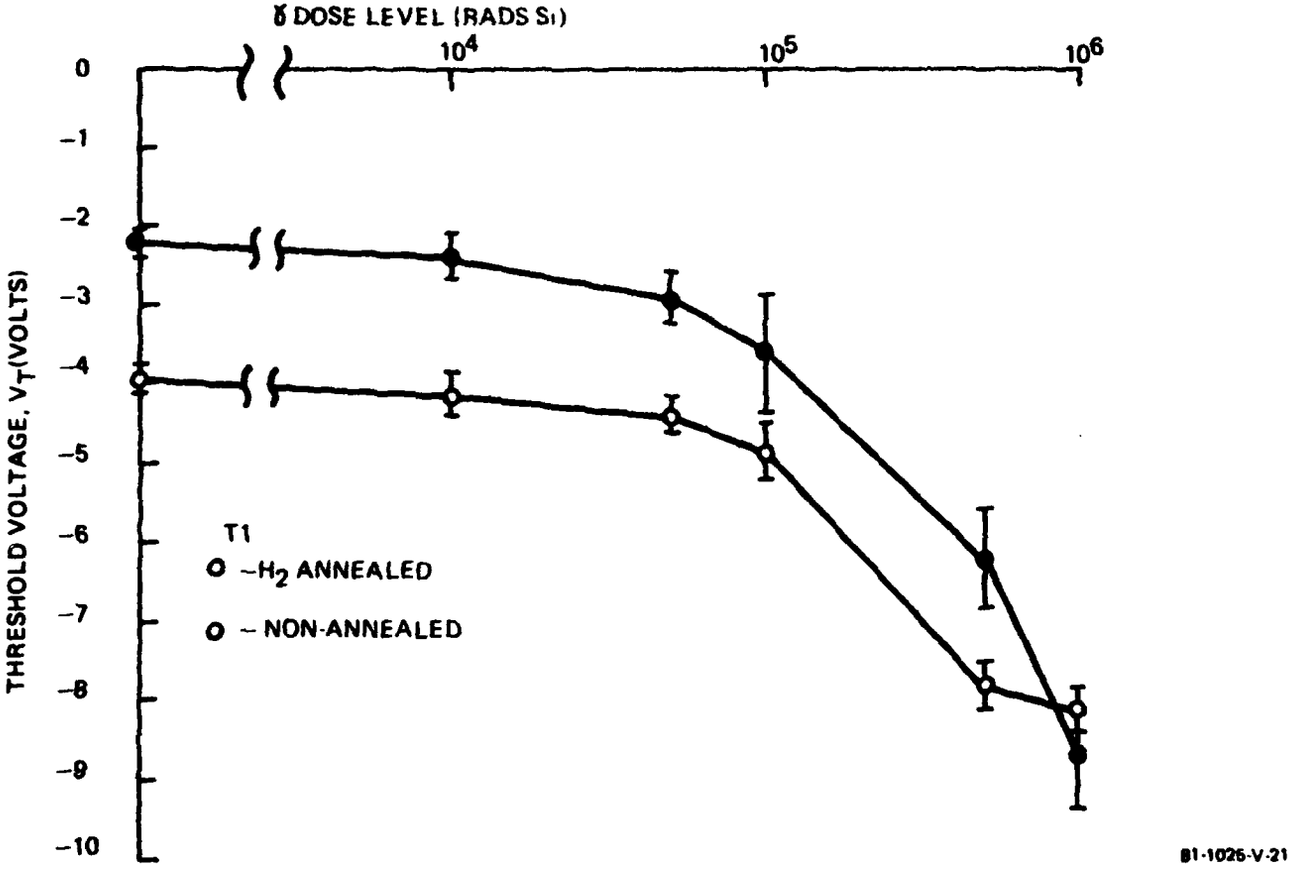


Figure 4-45. Threshold voltage as a function of total dose γ radiation dual dielectric; X_{ox} = 77A, X_n=1400A, V_{DS} = 0V, V_{GS}=-12V.

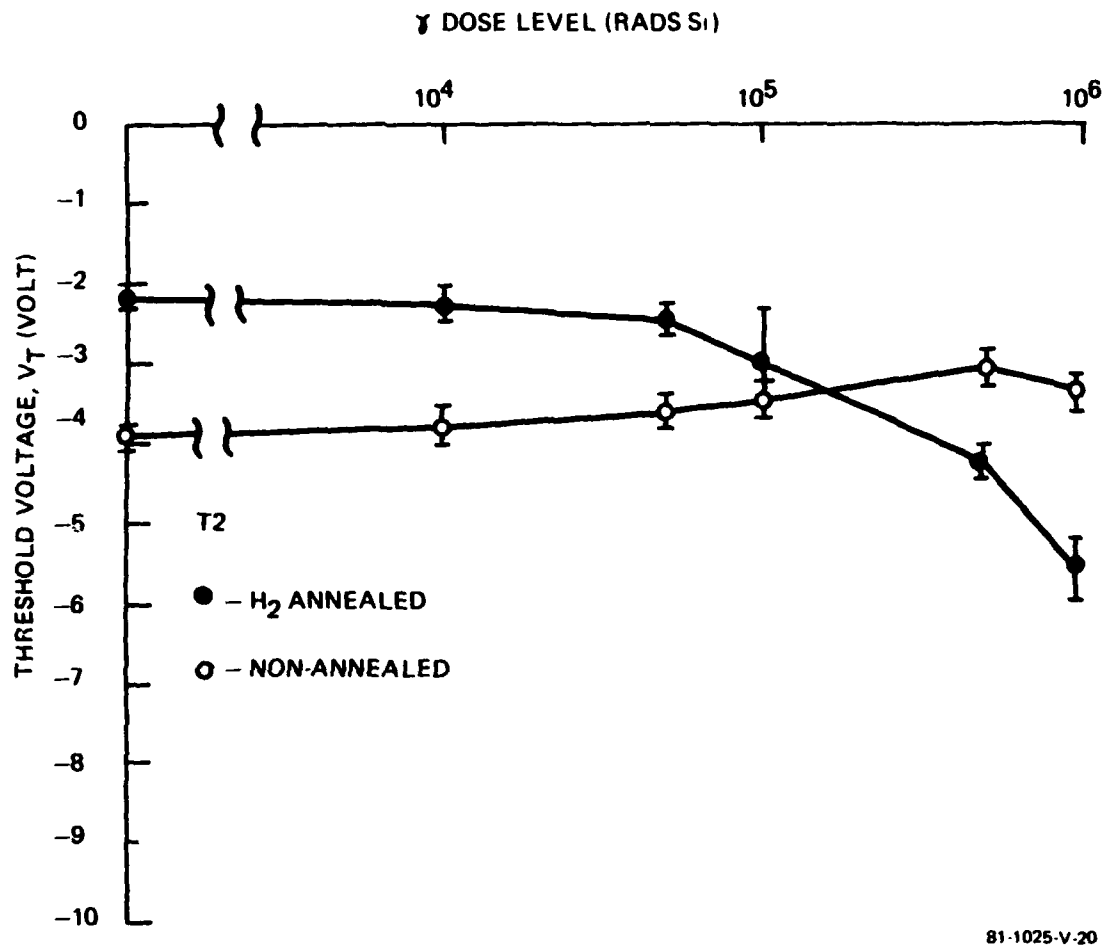


Figure 4-46. Threshold voltage as a function of total dose γ radiation dual dielectric, X_{ox}=77A, X_n=1400A, V_{GS} = 0V, V_{DS} = -20V.

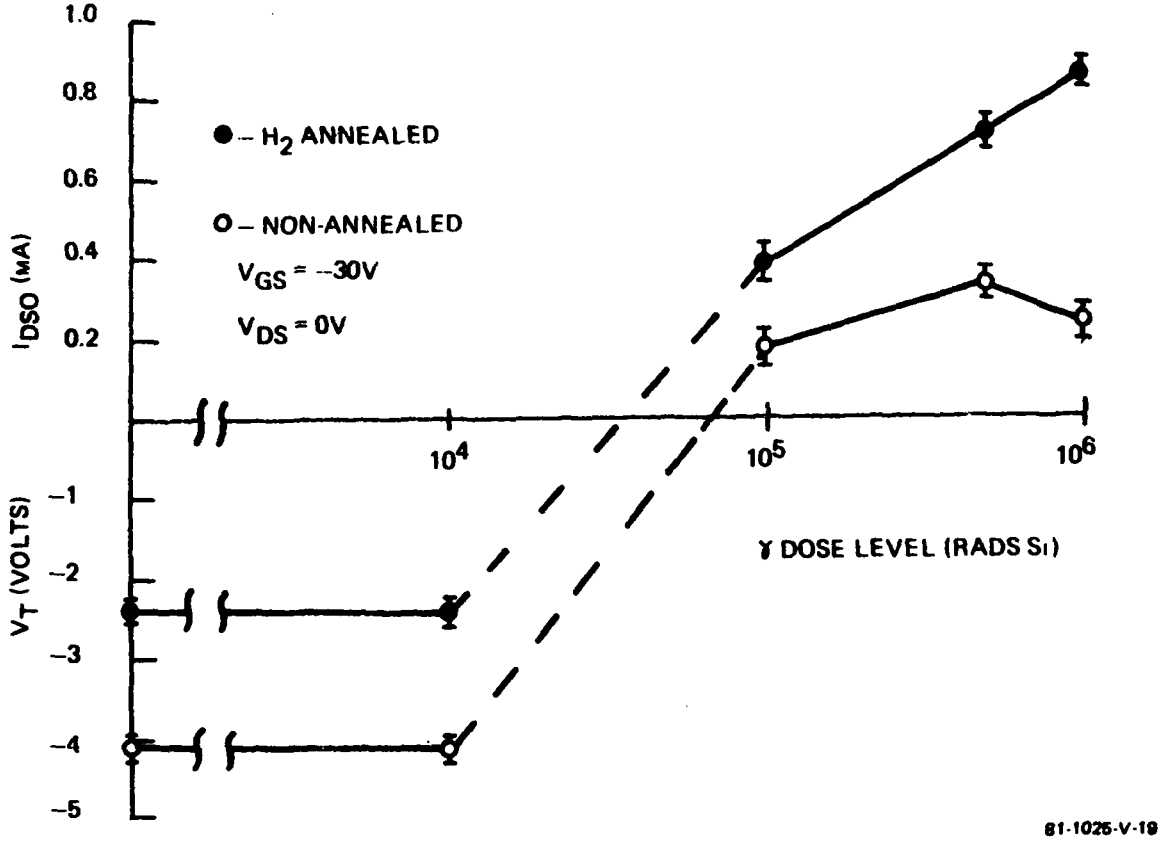


Figure 4-47. Threshold voltage and I_{DSO} as a function of total dose γ radiation. Dual dielectric; X_{ox}=77A, X_n=1400A, V_{GS}=-30V, V_{DS}=0V.

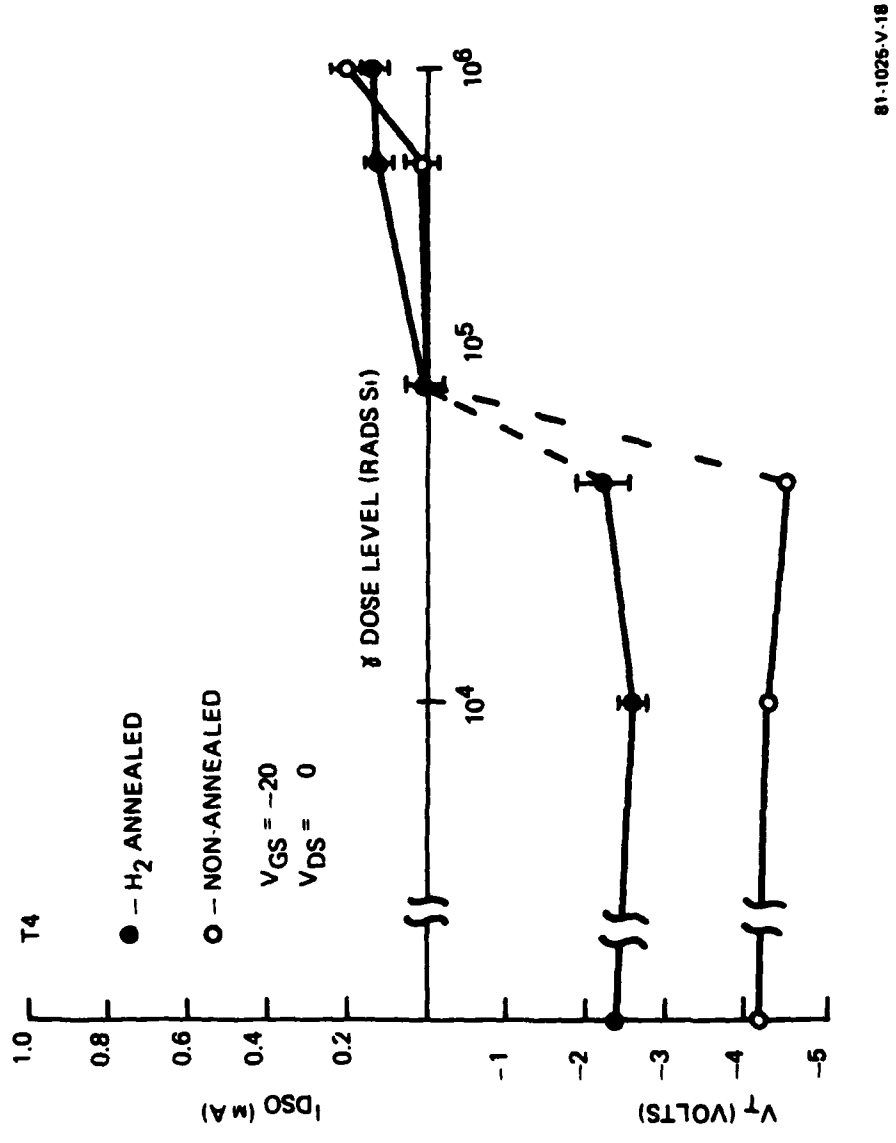


Figure 4-48. Threshold voltage and I_{DSO} as a function of total dose γ radiation. Dual dielectric; X_{ox}=77A, X_n=1400A, V_{GS}=-20V, V_{DS}=0V.

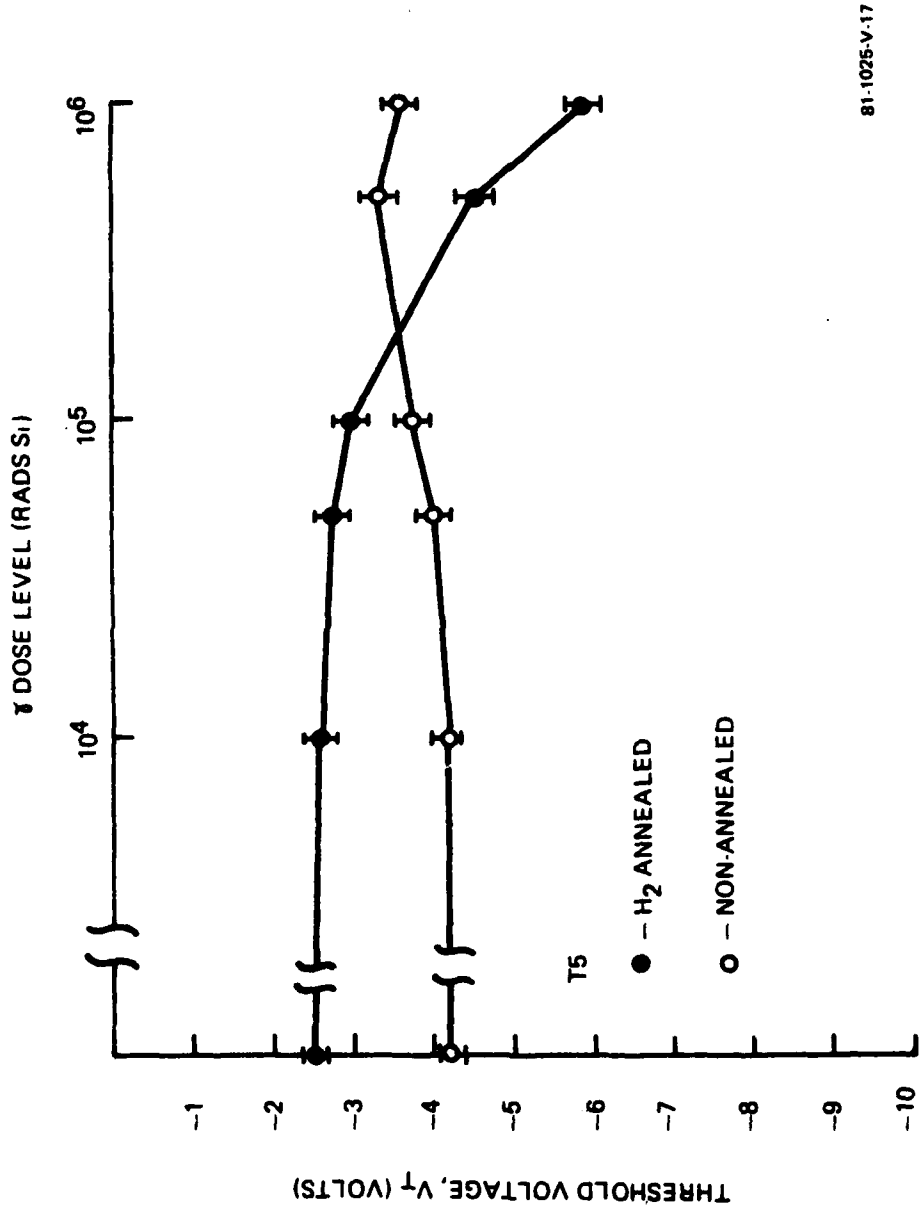


Figure 4-49. Threshold voltage vs total dose γ radiation dual dielectric: X_{ox}=77A, X_n=1400A, V_{GS}=0V, V_{DS}=-30V.

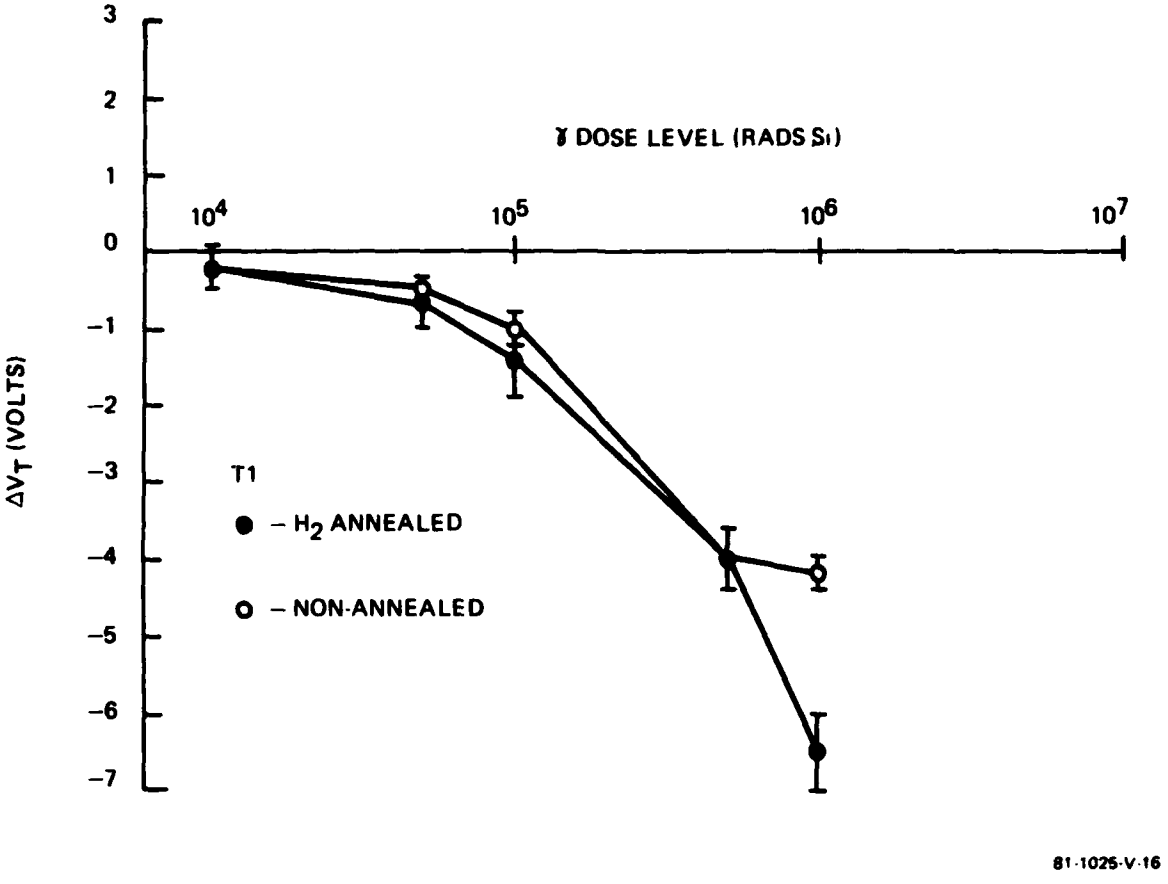


Figure 4-50. Change in threshold voltage as a function of total dose γ radiation: Dual dielectric, X_{ox}=77A, X_n=1400A, V_{GS}=-12V, V_{DS}=0V.

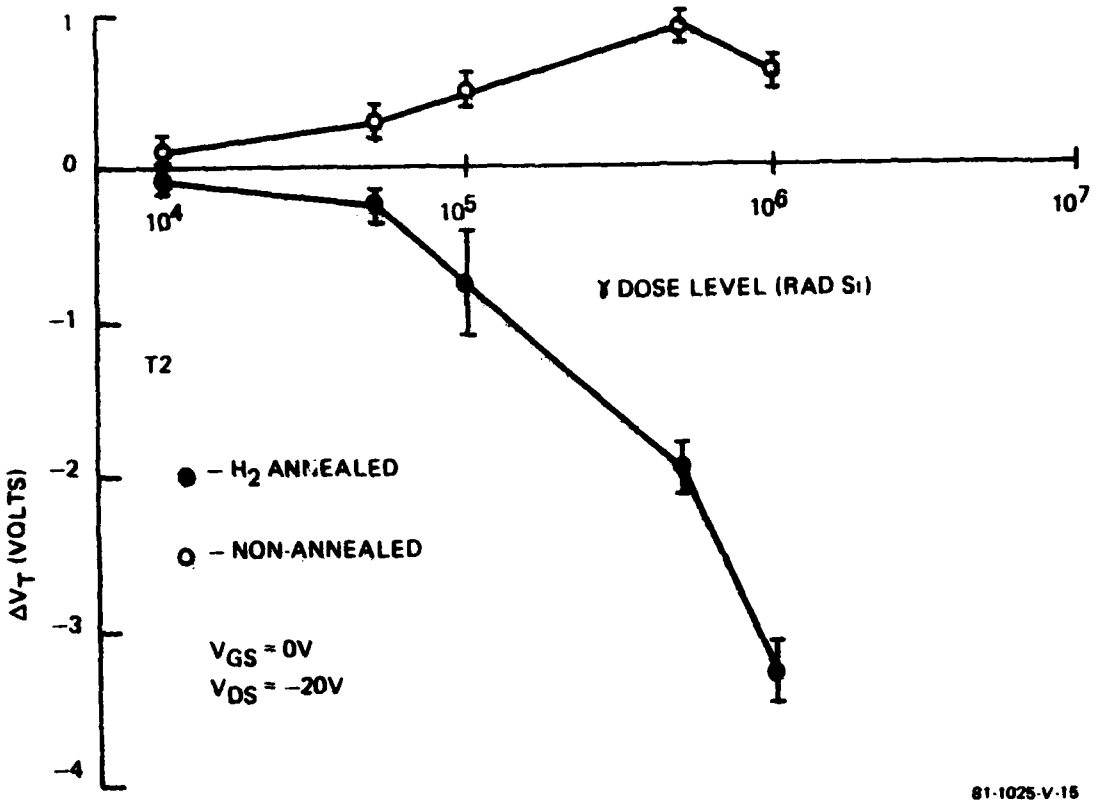


Figure 4-51. Change in threshold voltage as a function of total dose γ radiation. Dual dielectric: X_{ox}=77A, X_n=1400A, V_{GS}=0V, V_{DS}=-20V.

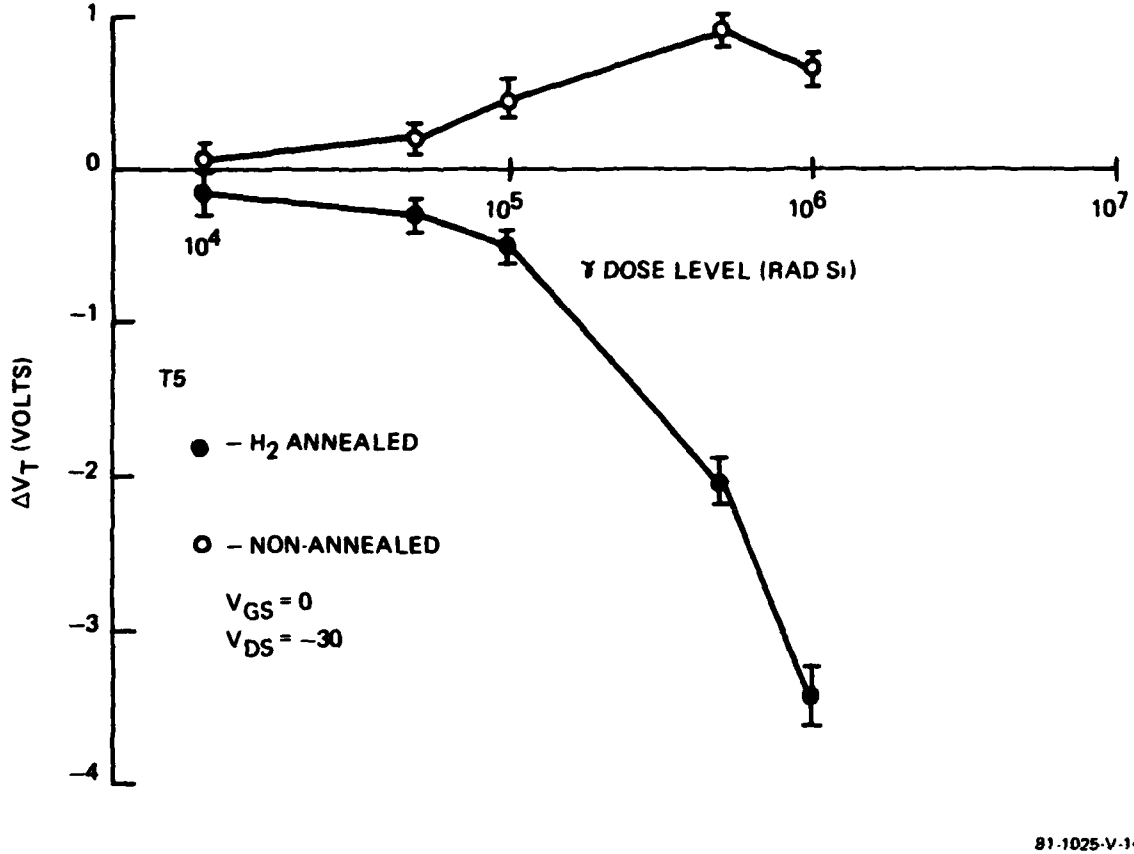


Figure 4-52. Change in threshold voltage as a function of total dose γ radiation. Dual dielectric structure: X_{ox}=77A, X_n=1400A, V_{GS}=0V.

occured between the drain-source bias level while the gate voltage was equal, V_{GS}=0. The similar variation in the threshold voltage between T2 and T5, suggests that no detectable changes occur when V_{DS} is changed from -20V to -30V, see Figures 4-51 and 4-52.

In Figure 4-47, the plots shows both H_2 annealed devices and those structures that were not annealed going into depletion at the 50K rad total dose level. Here, V_{GS}= -30V and V_{DS} =0. The biasing configuration with V_{GS} = -20V and V_{DS}=0V (T4), caused the devices to go into depletion at a 100K rad total dose level. The degree to which the transistors goes into depletion is larger for the condition of T3 than for T4. From the results given in Figure 4-50, it can be surmised that the devices that were H_2 annealed and those structures not receiving the anneal are affected in a similar manner for total dose radiation up to 1M rad. A shift of less than 2V was observed in the threshold voltage for structures biased wth V_{GS} = -12V and V_{DS} =0V (T1), to about 100K rads (Si), Figure 4-45. The slight positive shift in threshold voltage as a function of total dose radiation for the devices that did not receive an H_2 anneal and biased using the configuration of T2 and T5 is shown in Figure 4-51 and 4-52. The threshold voltage of the H_2 annealed structures shift negative as the total dose radiation level increase and exceeds the 2V mark after 500K rads. The threshold voltage shift for the device not receiving a post nitride anneal did

not exceed more than 0.9V, which occurred at 500K rads.

4.6.3 All Oxide Polysilicon Gate Transistor Devices

Devices fabricated using two (2) gate oxide growth processes were evaluated as a function of total dose radiation. One oxide type was grown with a procedure involving a dry followed by a wet sequence with the final step an anneal in 100% N_2 (DWN). The second type oxide was grown with a wet followed by a dry sequence with a subsequent N_2 anneal (WND). The process sequence depicting the gate growth conditions are shown in Table 4-12. The thickness of the oxide films was 721A and 696A for the DWN and WDN sequence respectively. Structures with various channel lengths were tested, see Table 4-13. The response of these structures with total dose radiation level was observed to be independent of channel length, therefore the data that will be presented comes from one device, the transistor with a channel length of 10um i.e. device #5.

The gate bias condition were $\pm$20V, $\pm$15V, +5V and 0V. The source, drain and substrate were held at ground potential, 0V. The threshold voltage was measured to be the gate voltage necessary to cause a drain current of 1uA to flow when the drain was biased with +5V relative to the source.

Table 4-12. Process sequence for all oxide polysilicon gate transistor structures.

Oxidation

1. Dry - 25 min
   Wet - 10 min
   N_2 - 15 min
   900°C
   X_{ox} = 696A

2. Wet - 20 min
   Dry - 25 min
   N_2 - 15 min
   900°C
   X_{ox} = 721A

Polysilicon Deposition

X_P = 5KA

Polysilicon Doping

Phosphine
900°C

Nitride Deposition

LPCVD
NH_3:$SiCl_2H_2$ = 9:1
750°C

Reflow Anneal

100% N_2
1050°C
Time = 20 min

Post Deposition Anneal

100%
900°C
Time = 30 min

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Table 4-13. List of channel lengths evaluated for all oxide polysilicon gate transistor structures.

Device #	Channel Length
2	4μ
3	5μ
4	6μ
5	10μ

Dry-Wet-N_2; DWN

Wet-Dry-N_2; WDN

The variation in threshold voltage as a function of γ total dose level is given in Figures 4-33 thru 4-58. All devices shifted in a negative direction as the dose level increased. Each of the structures that had a non-zero gate bias shifted into depletion at a relatively low dose level. The devices with WDN oxide gate degraded more severely with γ total dose radiation than did the films grown with the DWN sequence. Also, the positive bias degraded the structure much more severly than the negative bias.

Curves showing the square root of the drain current as a function of the gate to source voltage are given in Figures 4-59 and 4-60, for the WDN and DWN oxides respectively. $\sqrt{I_{DS}}$ is plotted as a function of V_{GS} for bias levels of 0V, -15V and -20V for the DWN film in Figure 4-61, and the WDN structure in Figure 4-62, after being subjected to a 2M rad total dose level. From these data it is observed that the threshold voltage variation is influenced by the lateral shift in the curves, (oxide charge and interface state build up), and the slope change (mobility degradation). Table 4-14 summarizes these where $\sqrt{\beta/2}$ has been calculated for the -20V, -15V and 0V bias level.

The suseptability to radiation damage by these structues is clearly apparent. However, the oxide grown with the DWN process was observed to be harder than the film grown

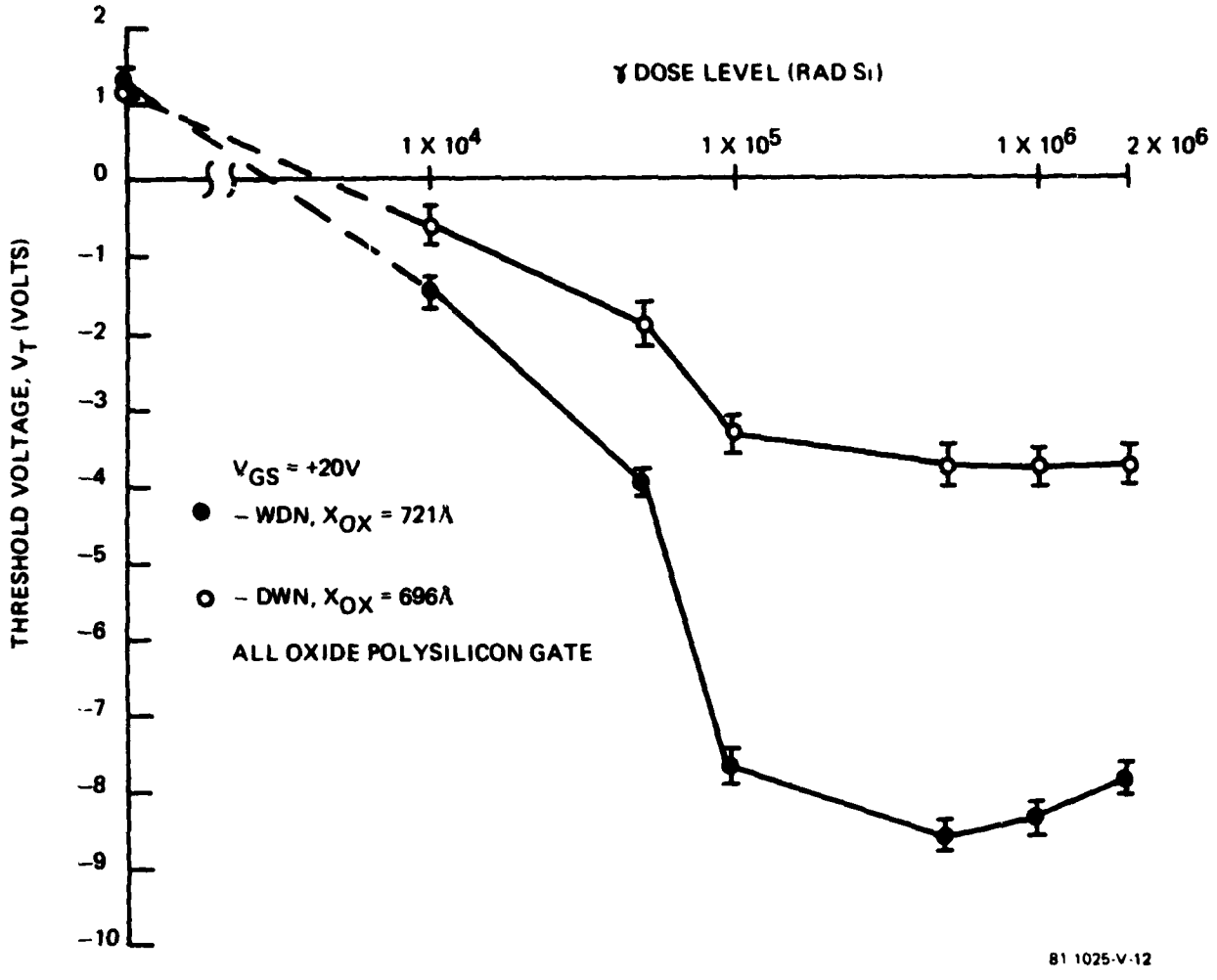

Figure 4-53. Threshold voltage vs. γ total dose radiation for all oxide polysilicon gate devices with V_{GS}=+20V.

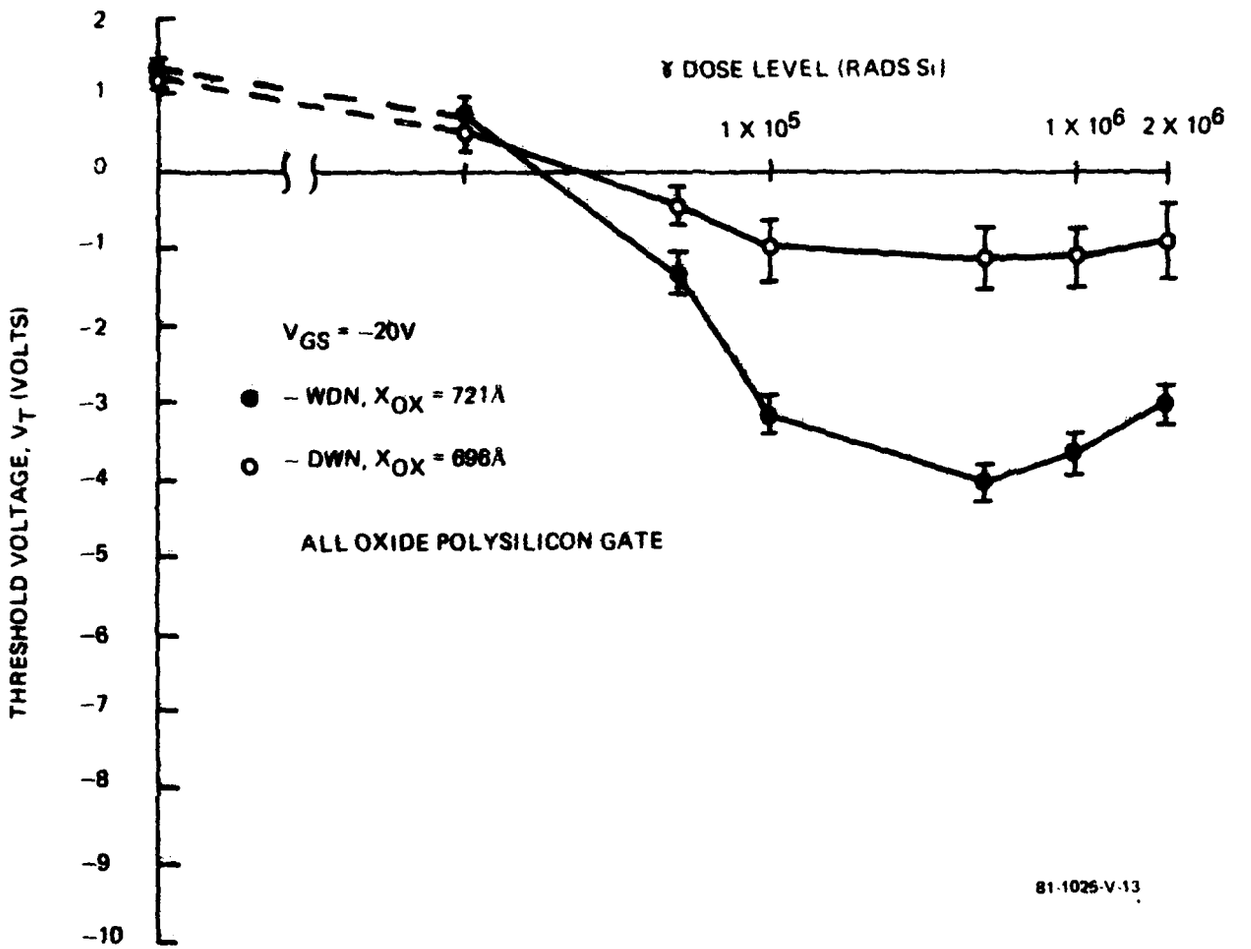

Figure 4-54. Threshold voltage vs. γ total dose radiation for all oxide polysilicon gate devices with V_{GS}=-20V.

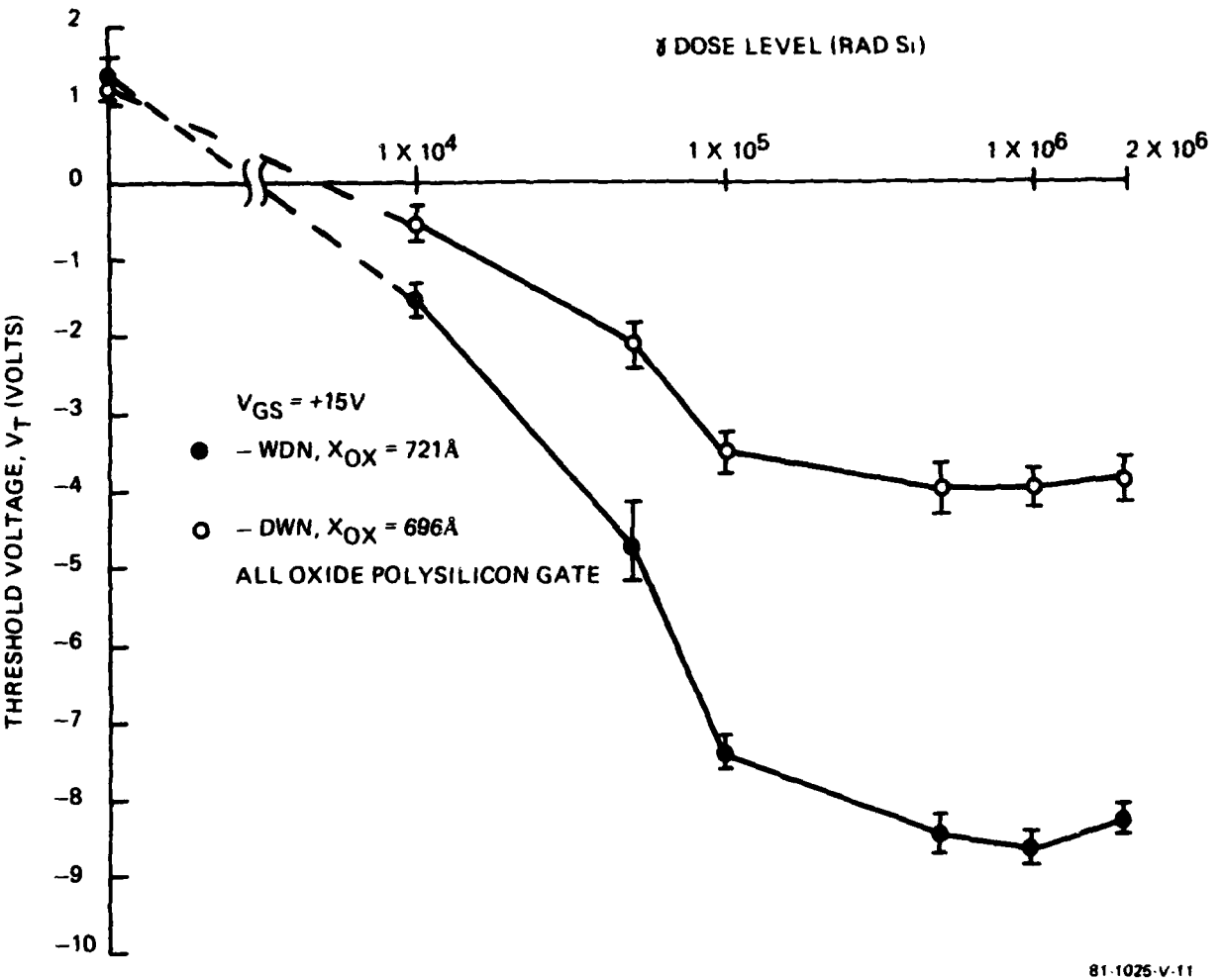

Figure 4-55. Threshold voltage vs γ total dose radiation for all oxide polysilicon gate devices with V_{GS}=+15V.

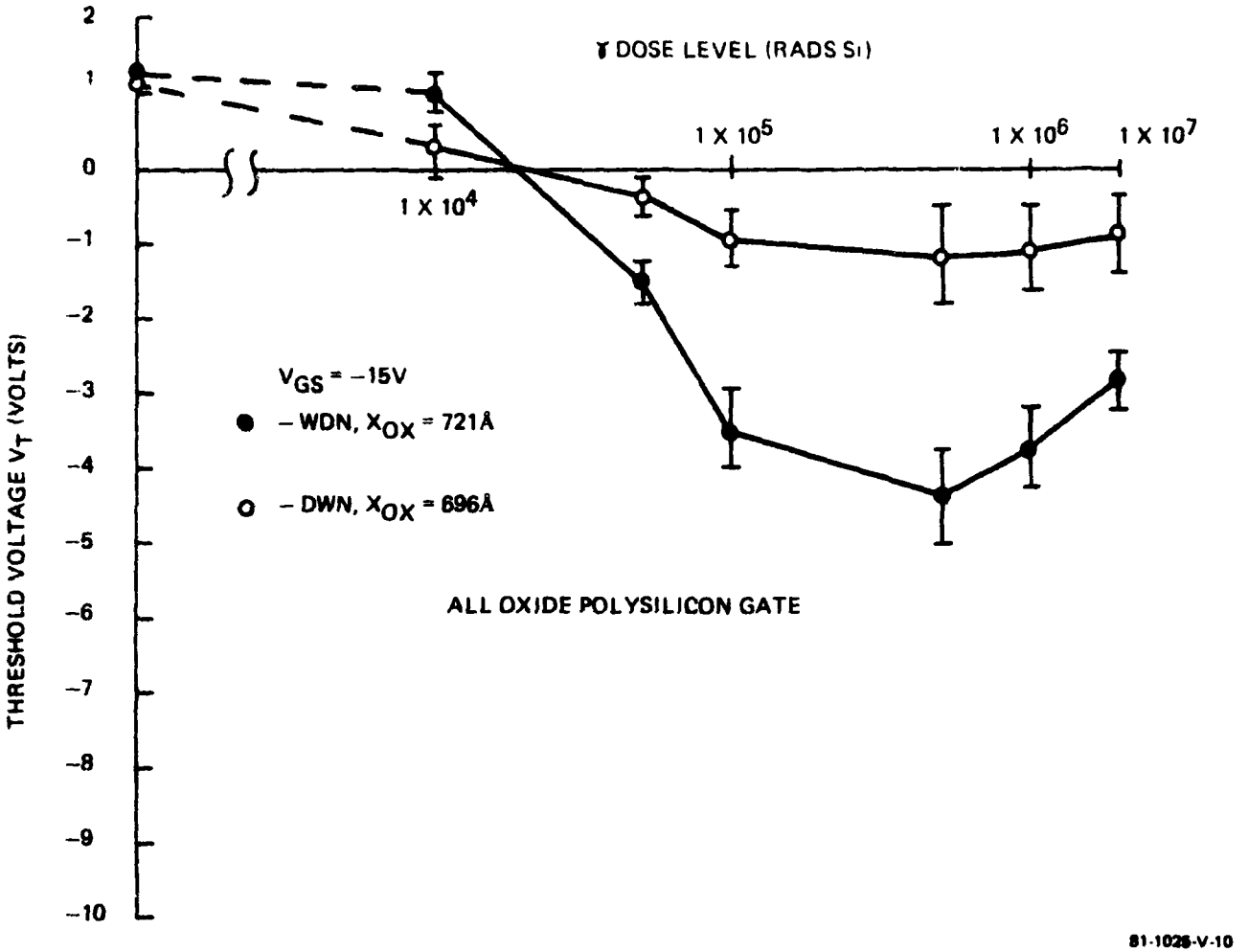

Figure 4-56. Threshold voltage vs γ total dose radiation for all oxide polysilicon gate devices with V_{GS}=-15V.

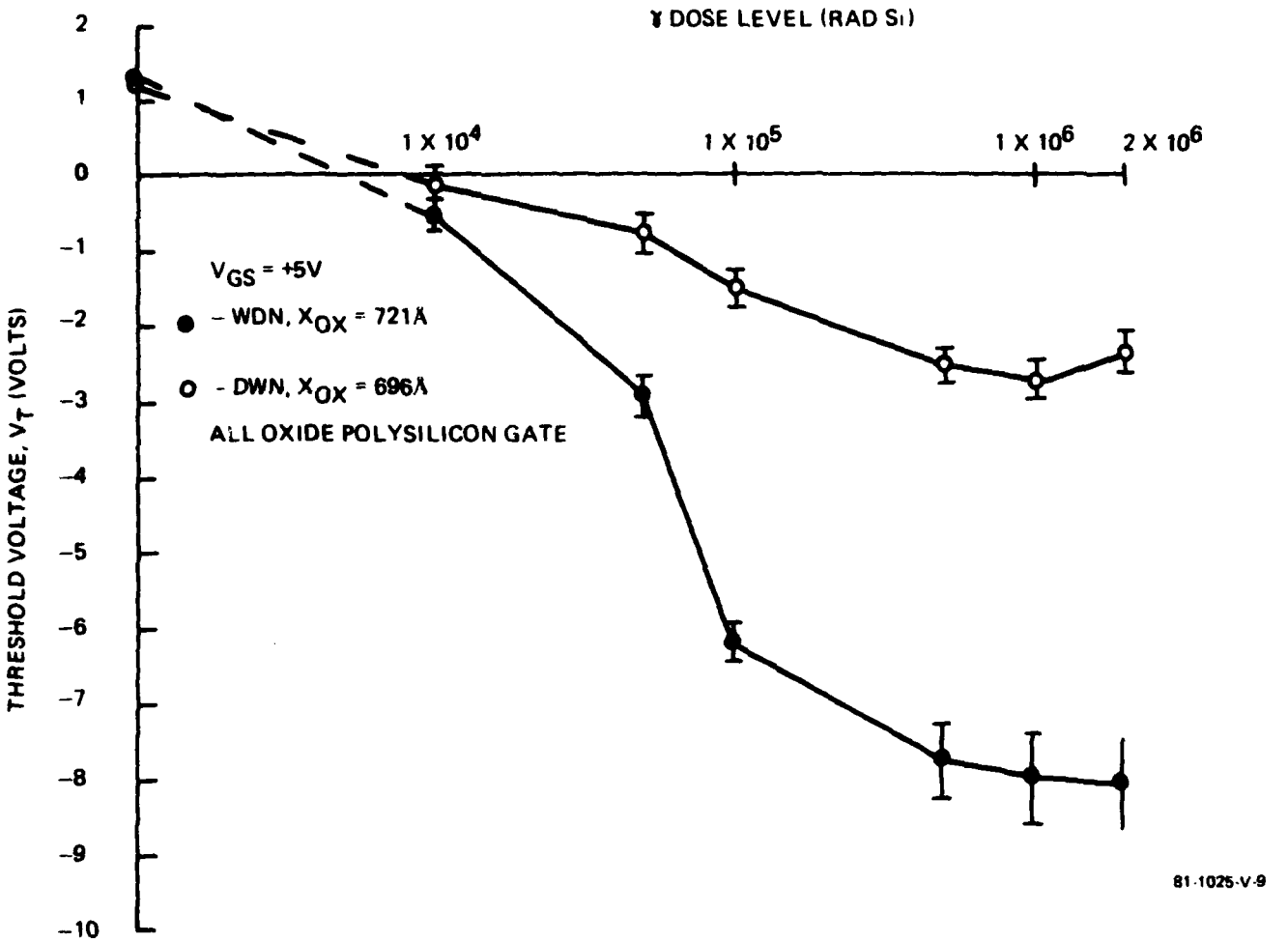

Figure 4-57. Threshold voltage vs γ total dose radiation for all oxide polysilicon gate with V_{GS}=+5V.

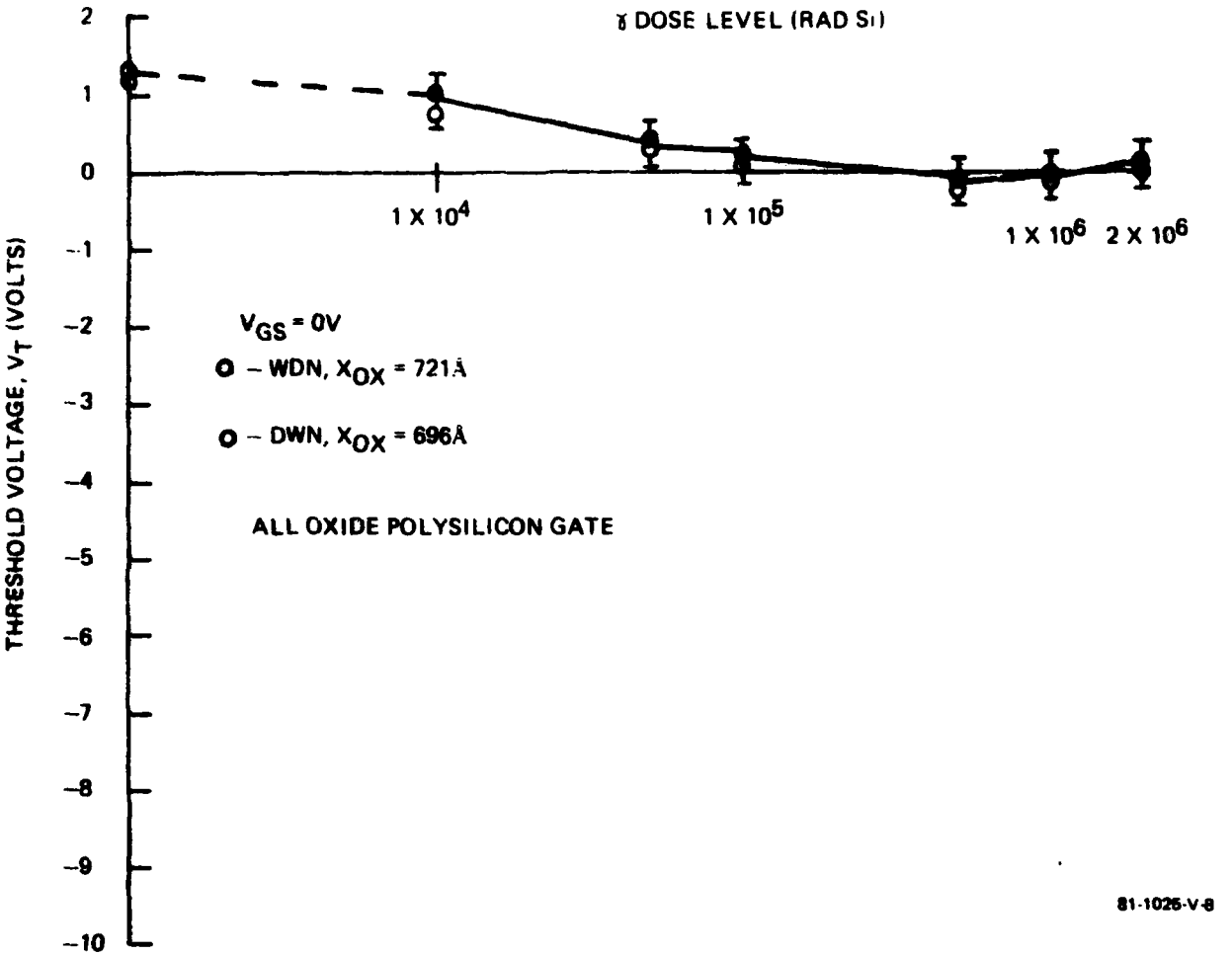

Figure 4-58. Threshold voltage vs γ total dose radiation for all oxide polysilicon gate devices with V_{GS}=0.

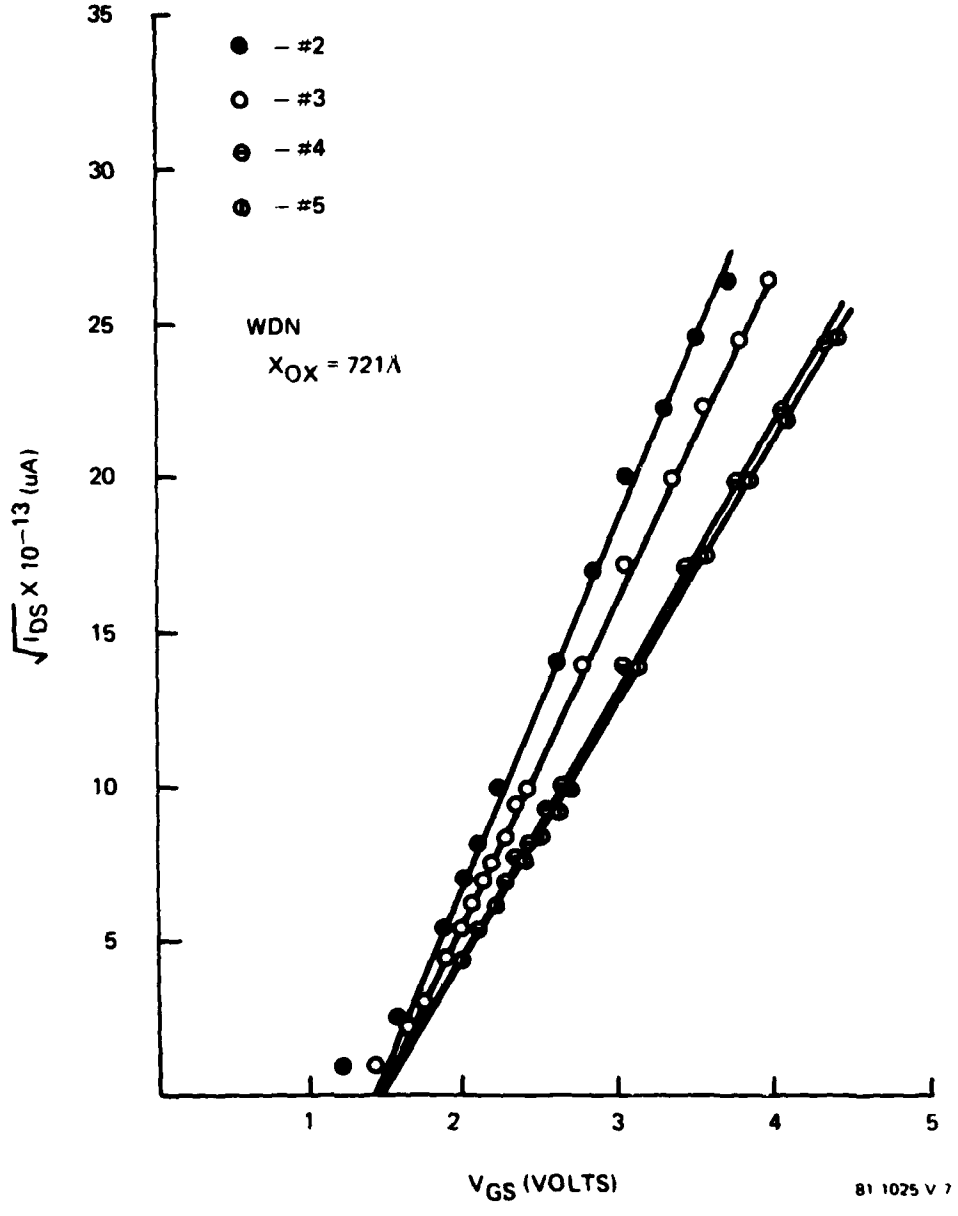

Figure 4-59. Drain/Source current vs. gate voltage for Wet-Dry-N_2 oxide.

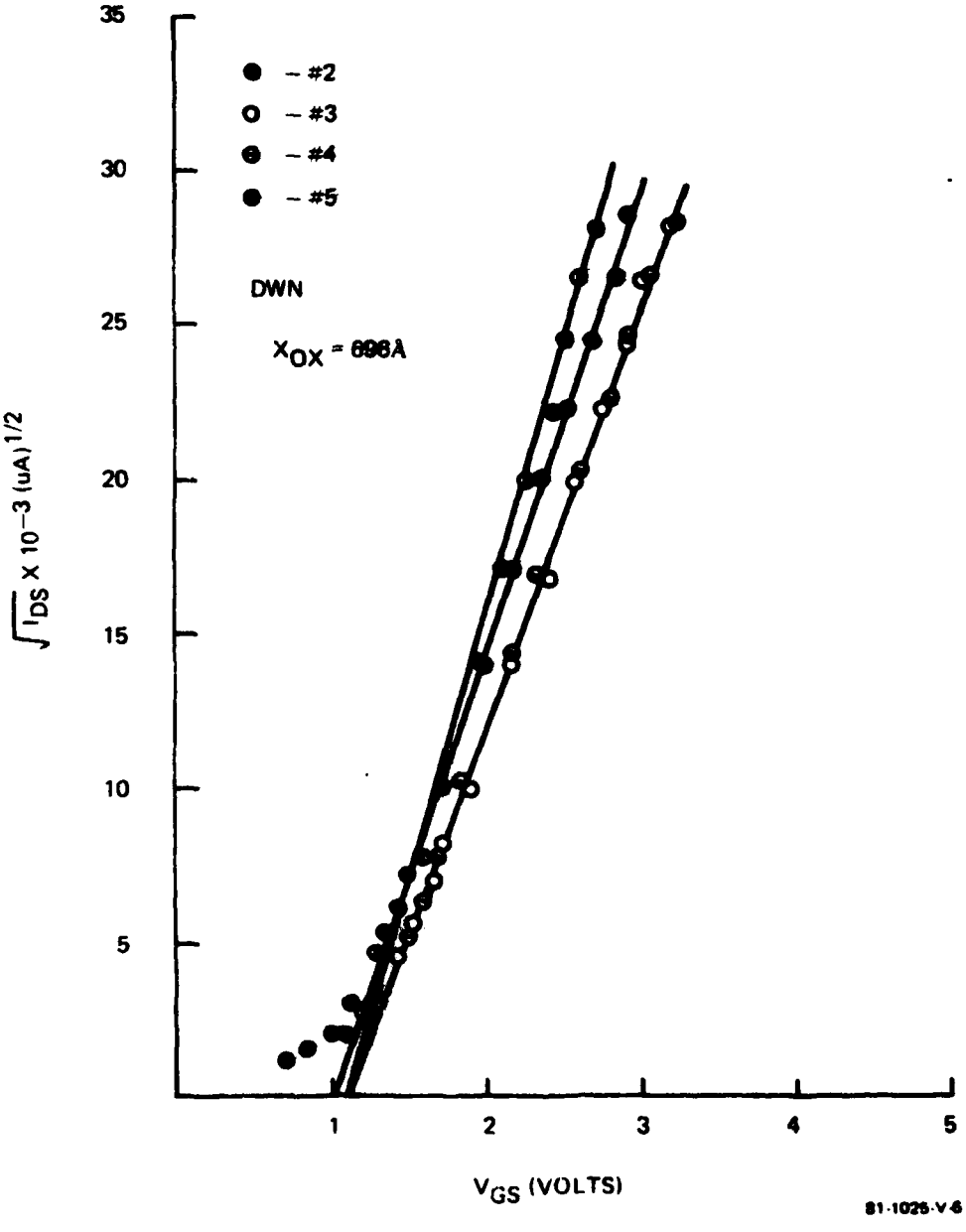

Figure 4-60. Drain/Source current vs. gate voltage for Dry-Wet-N_2 oxide devices.

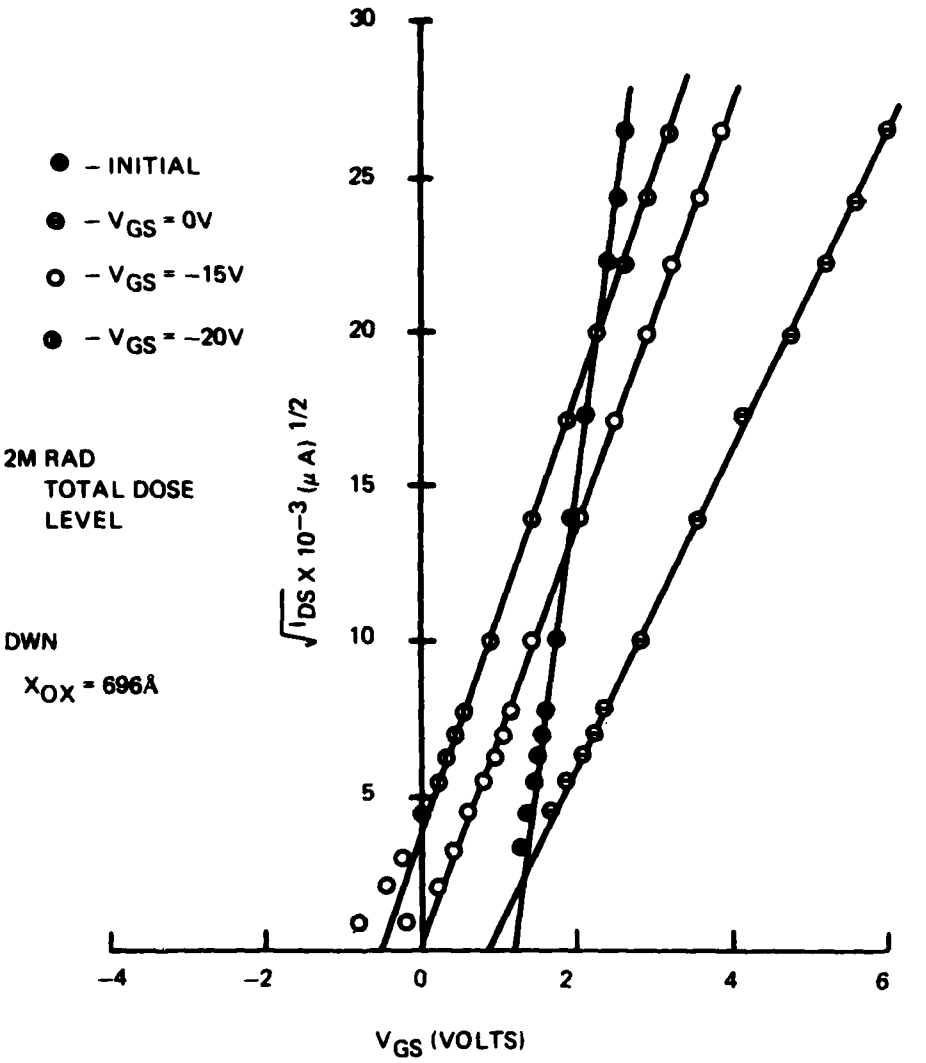

Figure 4-61. Drain/Source current vs. gate voltage for Dry-Wet-N_2 oxide devices after 2M rad total dose radiation.

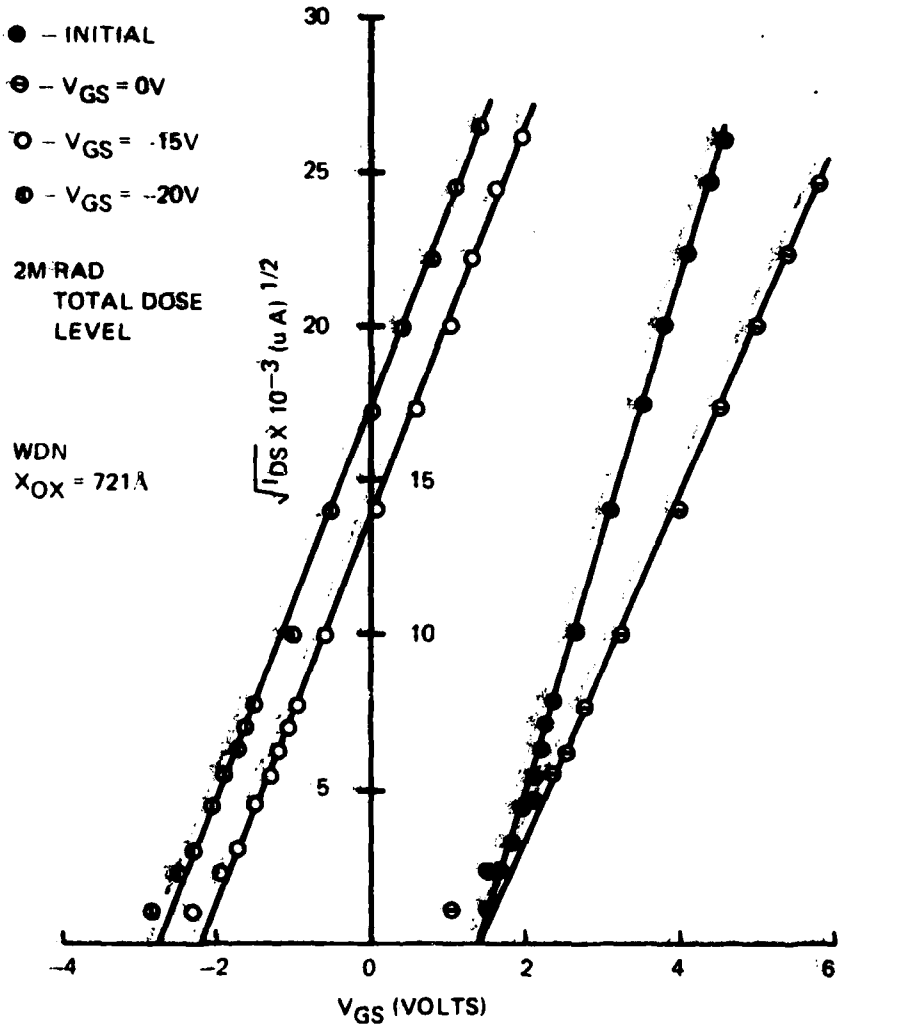

Figure 4-62. Drain/Source current vs. gate voltage for a Wet-Dry-N_2 after 2M rad total dose γ radiation.

Table 4-14. Variation in mobility and threshold voltage for different bias levels and oxide types at 2M RAD γ total dose radiation

DWN, X_{OX} = 696Å

BIAS LEVEL	$\sqrt{\beta/2}$	V_T
INITIAL	1.846×10^{-2}	1.46
−20V	7.010×10^{-3}	−0.58
−15V	6.932×10^{-3}	0.0
0V	6.358×10^{-3}	1.19

WDN, X_{OX} = 721Å

BIAS LEVEL	$\sqrt{\beta/2}$	V_T
INITIAL	8.377×10^{-3}	1.46
−20V	6.419×10^{-3}	−2.70
−15V	6.484×10^{-3}	−2.15
0V	5.637×10^{-3}	1.44

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by the WUN sequence. There is a 1050°C temperature step that each of the structures is subjected to subsequent to the gate oxidation at 900°C. The polysilicon was doped with a phosphorus doped glass. This technique must be evaluated with respect to hardness degradation. A number of variables have been identified that could be responsible for the hardness of these oxide e.g. the 1050°C reflow step and 900°C H_2 anneal. There are experiments currently being conducted that are directed at determining the extent that these variables influence the hardness of the oxide films.

4.6.4 P-Channel Un-protected memory structures

P-channel MNOS polysilicon gate memory transistors were fabricated and DC tested as a function of total dose radiation. The devices were biased with ±20V, ±15V, and 0V while being irradiated. The ±20V DC memory window was obtained for each condition subsequent to the respective dose levels. The threshold was taken to be the gate voltage necessary to cause 1uA of current to flow with a drain to source voltage of -5V. The memory nitride was deposited with an LPCVD reactor at 750°C with a NH_3:$SiCl_2H_2$ ratio of 9:1. The thickness of the film was 459A.

The ±20V DC memory window is given an a function of total dose radiation level in Figure 4-63. The memory window appears to increase slightly with radiation dose level. This

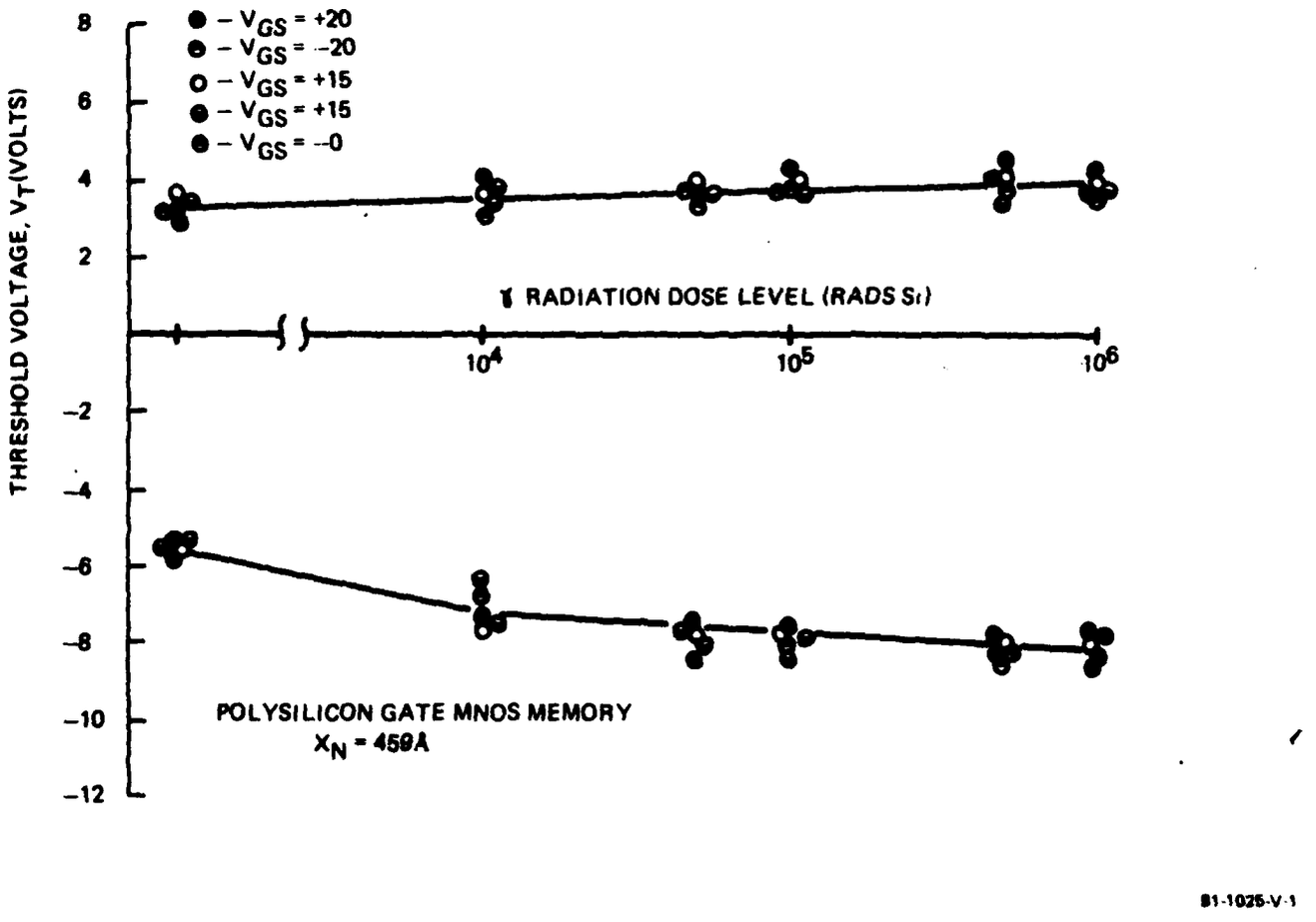

Figure 4-63. ±20V DC Memory Window vs total dose γ radiation for various bias conditions during irradiation.

could be related to the increase in window size observed with endurance cycling. The bias level did not have any influence on the DC behavior. Some degradation in the voltage decay rate was observed. The devices showed a 0.75 V/decade and a 0.5V/decade decay from -20V and +20V DC state respectively. See Figure 4-64. The initial decay rates were observed to be 0.6V/decade from the -20V state and 0.45/decade from the +20V level.

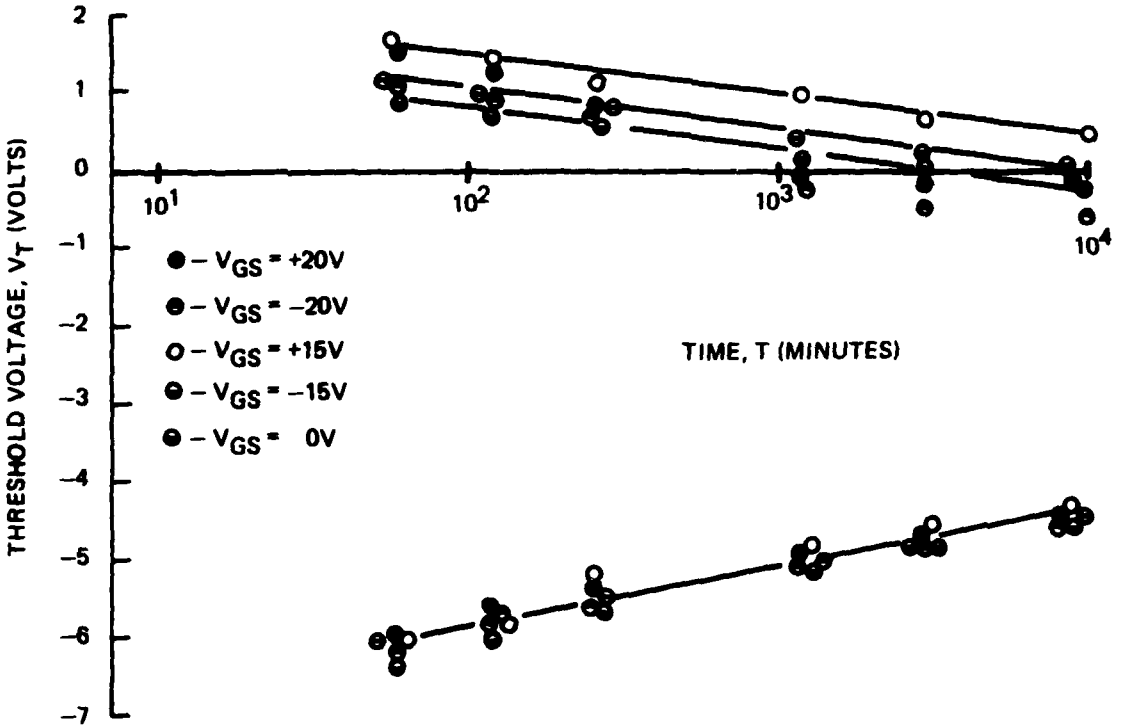

Figure 4-64. Voltage decay after exposure to 1M radiation total dose level. From ±20V DC state, at various bias levels.

81-1026-V-2

5.0 DISCUSSION

The average trapping length, X_o, the steady-trapped charge density, $n_t^{st}(0)$, and the minimum trap density, N_{tm} were determined for both APCVD and LPCVD nitride films deposited with various NH_3:SiH_4 and NH_3:$SiCl_2H_2$ ratios respectively. These parameters are determined by realizing that the slope of Q_n vs $\bar{d}$ curves (See Figure 4-3), for small Q_n is given by:

$$\partial Q_n / \partial \bar{d} = 4qN_t n_t^{st}(0) / (2N_t - n_t^{st}(0)). \qquad 5\text{-}1$$

Hence, the minimum trap density is obtained by letting $n_t^{st} = N_t$ in equation 5-1 giving

$$N_{tm} = (\partial Q_n / \partial \bar{d}) / 4q \qquad 5\text{-}2$$

The trapping length is determined from the intercept of the Q_n vs d curves with the d axis, while the trap capture cross section is given by:

$$\sigma_t = 1/N_t X_t \qquad 5\text{-}3$$

The trapped hole and electron density, capture cross section and trapping length were obtained for temperatures of 25, 70 and 175°C, for an LPCVD silicon nitride with a NH_3:$SiCl_2H_2$ ratio of 9:1. The values of $n_t^{st}(0)$ were 8.3, 2.9 and 2.03 x $10^{18}cm^{-3}$ for electrons and 1.9, 1.72 and 1.57 x $10^{18}cm^{-3}$ for holes for the respective temperatures 25, 70 and 175°C. The associated trapping lengths were 53, 105 and 160A for electrons and 99, 110 and 120A for holes. As the temperature increased from 25 to 175°C, the trapping length for holes increased less rapidly than for electrons. The trapping length for holes is larger than for electrons below 125°C, while above this temperature the trapping length of electrons becomes larger. Thus, scaling is a function of the trapped charge species and is controlled by holes at temperatures below 125°C and electrons above this temperature. A calculation of the minimum thickness of

dielectric needed to trap an arbitrary density of charge of $1uC/cm^2$ (See Figure 4-3), and assuming a scaling limit indicated by the condition that $X_n \geq 2\bar{d}$, shows that a minimum nitride thickness of 480A is required at 175°C. At 125°C this value reduces to 300A, and becomes 260A at 25°C.

The density of trapped charge decreased as the NH_3:SiH_4 ratio increased for APVD films, and as the $NH_3SiCl_2H_2$ ratio increased in the LPCVD structures, see Figure 4-1. The trapping length increased and trap capture cross section decreased as the gas ratio was increased. With an increased trap density and decreasing trapping length, a relatively fast write pulse response would be expected from such films. As shown in Figure 4-5 the pulse response of the 28:1 NH_3:SiH_4 (APCVD) film is larger for nitride fields values $\leq$ 4.5 MV/cm. However, for larger field values, the behavior becomes rather complex. The poor pulse response observed above 4.5 MV/cm can be explained on the basis of a detrapping phenomena where charge detrapping is due to the electric field in the charge free region of the silicon nitride. As the charge centroid propagates into the silicon nitride, the field in the charge free region of the film increases, causing eventual detrapping at the leading edge of the centroid. These detrapped charges can be trapped deeper into the nitride or migrate to the gate forming a conducting current. The final result is that the charge spreads deeper into the film, which in effect influences the flatband voltage shifts given by:

$$\Delta V_{FB} = \Delta Q_n \left(X_n - \bar{d} \right) / \varepsilon_n \qquad 5\text{-}4$$

From equation 5-4 it is seen that incrasing the charge centroid acts to decrease the flat band voltage shift. Thus, when the spreading of the charge in the nitride is such that the effect of its centroid growth cancel the effect the trapped charge has on the flatband voltage, the device saturates, or the flatband voltage shift reaches a maximum value. When the depth of the centroid becomes such that it overcompensates for the injected trapped charge, the flatband voltage will experience a turn-around, i.e. for voltages larger than that which is needed to produce the maximum or saturated value, will cause a flatband shift smaller than the saturated value. This would occur at relatively low field levels in high conductive film, since detrapping is expected to occur at relatively low fields. The largest flatband voltage shift or memory window size was not produced by films with the highest NH_3:SiH_4 ratio investigated, (450:1). The saturated value was lower than for either a 300:1 or 150:1 ratio films at nitride field value > 4.5MV/cm. The behavior can be explained by realizing that the trapping length of the films increases as the

NH_3:SiH_4 ratio increases and the density of the trap charge decreases. Again, as the charge centroid increases, the field in the charge free region of the nitride increases to the point where detrapping is initiated and the charge spreads deeper into the film, until eventually the flatband voltage shift saturates. Because the trapping lengths of the high NH_3:SiH_4 ratio films are relatively large, the amount of charge trapping that will produce a centroid large enough to cancel the effect of the trapped charge is less than that which would be needed for a film with a lower NH_3:SiH_4 ratio. Consequently, the field at which the flatband voltage shift saturates for a film with an NH_3:SiH_4 ratio of 450:1 is less than a nitride deposited with a NH_3:SiH_4 ratio of 300:1. The curves in Figure 4-5 show that the optimum NH_3:SiH_4 ratio for a lusec pulse width occurs between 28:1 and 450:1.

In an effort to produce a dielectric that has a relatively fast pulse response and gives an appreciable memory window size, a dual dielectric structure was fabricated. The gate structure consisted of a high conductive film deposited as the first layer to enhance the pulse response with a low conductivity film as the second layer to prevent excessive spreading of the charge centroid thereby reducing the charge decay rate as well as improving the memory window size. The pulse response of the structures were obtained for electron

injection. The pulse widths ranged from lusec to lmsec. The initial field across the nitrides ranged up to 7.5 MV/cm. These field values were calculated using the following relationship.

$$E_{no} = V_g / X_n^{eff} \qquad 5\text{-}5$$

V_g is the applied gate bias and,

$$X_n^{eff} = X_{n2} + X_{n1} + (\epsilon_n / \epsilon_o) X_{ox}$$

X_{n2} is the tnickness of the second layer nitride, X_{n1} the thickness of the first layer nitride, X_{ox} the oxide thickness ($\approx$ 20A) and $\epsilon_n / \epsilon_o = 1.667$. The saturated memory window increased from about 3.0 volts in the case of the single layer APCVD nitride with an NH_3:SiH_4 ratio of 28:1, to about 5.5 volts when the two step structure was used which consisted of a 28:1 APCVD first layer and the second layer containing an LPCVD film with a NH_3:$SiCl_2H_2$ ratio of 9:1. The structure in which the first layer was an LPCVD film with a NH_3:$SiCl_2H_2$ ratio of 3:1 and the second a 9:1 LPCVD film saturated at about 4.5 volts. For fields $\geq$ 4.5 MV/cm and a lusec pulse width, the pulse response of the two step

structures were comparable to the low conductivity film. Thus, in this field range, the pulse response is controlled by the higher conductive layer nitride.

By exposing "very thin" layers of memory nitrides to various gas ambients at elevated temperatures, it is reasonable to expect that the tunneling parameters at the nitride oxide interface will be altered. Thin films (29A and 51A) of LPCVD 9:1 silicon nitride were annealed in either N_2, H_2 or NH_3, over which a 391A LPCVD 9:1 film was deposited. The second layer was either annealed in H_2 or did not receive any anneal, see Table 4-7. The devices that were annealed in N_2 and whose first layer consisted of a 51A film showed the superior pulse response characteristic for each pulse width investigated, (1usec, 10usec, 100usec and 1msec). Less than a 1 volt variations were observed in the pulse widths and anneal ambients. Figures 4-12 thru 4-14 depict these results. The interface state density (Table 4-8 and 4-9) was found to decrease by a relatively large percentage in structures that were annealed in NH_3. The H_2 does not appear to affect the interface state density, in particular when both layers receive the anneal. A correlation between the interface state density and the charge decay rate was realized in the 21A layer devices annealed in NH_3. Relatively low decay rates were found for both holes and electrons for the above treatments and gate structures. The decay rates of the remaining structures were similar, even for the devices with a 51A first layer that was

annealled in NH_3. It appears that some of the tunneling parameters at the oxide/nitride interface are being modified by the various annealed ambients. The H_2 anneal, however, affects primarily the bulk of the film and does not seem to alter the interface to any noticeable degree. This result was surmised because of the relative positve shift observed in the flatband voltage after H_2 annealing and the relative peak heights of the conductance - voltage curves. As much as a 2 volt shift in the $\pm$20V saturated flatband voltage and the center of the memory window occurred in the structures that were annealed in H_2 while the relative conductance - voltage peak height was 1.0, indicating a decrease in fixed positive charge in the structures with the interface state density remaining unchanged.

Temperature - Bias - Stress (TBS) tests were conducted on polysilicon gate non-memory capacitor structures. The two conditions consisted of a polysilicon before memory nitride and a polysilicon after memory nitride process. The oxide dielectric was a dry-wet-dry film grown at 900^{o}C to a thickness of 800A. The polysilicon after memory nitride process yields an all oxide gate structure while the polysilicon before memory nitride produces an oxide/nitride structures with an 800A oxide over which the memory nitride ($\simeq$ 400A) is deposited. The structures were stressed with a $\pm$20V DC bias at temperatures of 25^{o}C and 200^{o}C. Both gate structures were shown to be quite stable, as is shown in

Table 4-5. The DC memory window of the polysilicon after memory nitride process is shown in Table 4-6 to be comparable to the metal gate structures. In the polysilicon gate process, the memory nitride is oxidized to prevent charge injection from the polysilicon, (holes for a positive gate bias and electrons for a negative gate bias), while the polysilicon was oxidized to guard against possible side effects. It was surmised from the results given in Table 4-5, that a small amount of phosphorous probably diffuses through the 3.6KA polysilicon and tails into the oxide. More appears to be penetrating from the doped glass sources than for the phosphine. It should be noted, however, that the drive times for the doped glass source procedure were longer than for the phosphine source.

With these results, subsequent polysilicon gate capacitor structures of this type were doped with the phosphine source, even though each doping source and drive time produced stable gate structures.

D-C memory window, pulse response, endurance and retention measurements were conducted on a metal gate MNOS/SOS test vehicle. The 6023T test pattern provided a number of memory subcells of various sizes. The subcell studied consisted of four memory transistors connected up the same way as they would be in a permanent memory array. The lay out of the structures are such that four of the subcells can be placed in a 16 pin DIP for measurements and testing. The endurance cycling was

accomplished with a driver circuit designed by inhouse personnel. Pulse response, retentivity and memory window measurements were performed on a macrodata 154 test unit.

The memory nitride structures were varied according to the following:

(1) 429A APCVD, $NH_3:SiH_4$ = 28:1

(2) 143A APCVD, $NH_3:SiH_4$ = 28:1 + 244A LPCVD, $NH_3:SiCl_2H_2$=9:1

(3) 374A LPCVD, $NH_3:SiCl_2H_2$ = 9:1

Each of the above structures received an additional treatment, that being an oxidation in steam at 900°C, followed by an H_2 anneal for 1 hour at 900°C. From this point forward the structures will be referred to as annealed or non-annealed with annealed meaning that the film has been subjected to the above post heat treatment. The transistors have the drain-source protected (DSP) structure. This means that the positive shift of the memory cell is limited by the threshold voltage of the non-memory devices that are part of the structure.

The large negative threshold voltage values observed in the devices that were non-annealed (See Table 4-2), indicate that an appreciable amount of fixed positive charge is present in these nitride structures, with the largest amount found in the single layer APCVD film. The memory window size of the single

layer APCVD structure and the two step structure, which consisted of an APCVD layer over which an LPCVD film is deposited, were 4.0V and 4.08V respectively for the non-annealed conditions. The window size of the LPCVD film receiving the same process treatment was 3.74V. The similar values obtained for the memory window sizes in the single layer APCVD structure and the dual layer or two step structure suggests that the oxide nitride interface and trapping parameters of the dielectric are also similar. This result infers that the memory characteristics of the two step structure of this type will be controlled by the highly conductive first film. It was noted earlier that the fixed positive charge could be decreased in a nitride by post deposition annealing in H_2 at 900^{o}C. The manifestation of this phenomena is realized when the capacitor structures that have received a post H_2 anneal experience a postive shift in the flatband voltage relative to the non-annealed devices. The same effect is demonstrated in the present structures by the positive shift in the threshold voltage of the non-memory devices, and the center of the memory window, of a H_2 annealed structure relative to a similar non-annealed device.

The DC memory window size of the H_2 annealed devices were consistently larger than that of the non-annealed structures. An increase of 1.57 volts was produced in the single layer APCVD nitride, 0.55 volts for the dual layer two step structure and 1.51 volts for the singler layer LPCVD film. Non-memory

threshold voltage changes from -7.5V to -3.85V = 3.65V, -6.5V to -4.23V = -2.27V and -5.98V to -2.86V = 3.12V for the single layer APCVD, two step structure, and single layer LPCVD nitride films respectively were produced by H_2 anneals at 900°C. From these results the following effects were attributed to the H_2 anneal,

(1) The amount of fixed positive charge in the nitride was decreased.

(2) The center of the memory window shifts positive.

(3) The DC memory window size is increased.

The relative integrity of the dielectrics was based on the number of subcells taken from identical areas of the wafers that functioned properly out of a sample size of 24. The devices that showed the lowest degree of functionality contained the APCVD film that was annealed in H_2. The LPCVD nitride that was annealed in H_2 appeared not to have experienced this failure mechanism. The most common mode of failure was the gate starting to conduct relatively high currents at low voltages, between 0.5 to 5.0V, when the devices were attempted to be written or cleared. Note that the similar degree of failure experienced by the two device structures that contain an APCVD layer that was annealed in H_2 further suggests that the memory characteristics of these two layer

structures are controlled by the first layer, i.e. the APCVD (28:1) film. The above results tend to indicate that the H_2 anneal degraded the integrity of the APCVD films.

The memory subcells were endurance stressed by applying a repetitive simulated C/W voltage wave between the transistors gate and source-drain-substrate connected together. The following field levels and pulse widths were used to stress the devices.

t_w = 100usec, E_n = 5 MV/cm
t_w = 1usec, E_n =6 MV/cm
t_w = 1usec, E_n = 7 MV/cm

The Macrodata 154 programs that were used to test the devices, functioned in the following manner:

Program 1. Apply $\pm$20V for 1 sec to the gate and measure the threshold voltage for the written and cleared states.

Program 2. Apply a multiple number of 100usec $\pm$27V pulses and measure the threshold for the written and cleared states.
Apply a multiple number of $\pm$27 pulses followed by a -27V 100usec single pulse. Measure threshold at lapsed times of 1, 3, 10 and 30 seconds. The same procedure is repeated for opposite voltage polarities.

Program 3. Apply a multiple number lusec -29V pulses and measure threshold. Apply 10^5 cycles of lusec pulse width and amplitudes of +27V and -29V, and measure threshold.

Apply a lusec +27V pulse and measure threshold at lapsed times of 1, 3, 10 and 30 seconds. Apply a lusec -29V pulse and measure threshold at lapse times of 1, 3, 10 and 30 seconds.

The devices that were stressed with a 100usec pulse, were only cycled to 10^9 because of the time necessary to achieve the high number of cycles, i.e. about 3 days to reach 10^9 and a month to reach 10^{10} cycles. For the same reasons, the devices that were subjected to the lusec pulse widths were only cycled up to 10^{11}.

The DC memory window size was influenced by endurance cycling in the following ways.

A. X_n = 374A LPCVD nitride.

(1) $\pm$20V DC memory window is larger for the H_2 annealed devices when compared to the non-annealed case for each cycling condition. The nitride field stress was 5 MV/cm with a 100usec pulse width. See Figure 4-18 and 4-19. The window size of the H_2 annealed cells

measured about 4.5 to 5 volts, while the non-annealed structures measured between 3.5 to 4.5 volts, reaching its maximum value of 4.5V at 10^8 cycles.

(2) Between 10^8 and 10^9 cycles the memory windows of the devices that were not subjected to an anneal became larger than the devices that were annealed when stressed with E_n = 6MV/cm and t_w = lusec (Figure 4-22). The window sizes of the annealed structures again range between 4.5 and 5 volts while the non-annealed devices maintain a value of 3.5 volts from 10^6 to 10^8 cycles increasing to about 5.5V at 10^8 cycles and maintaining this level up to 10^{11} cycles.

B. X_n = 143A APCVD + 244A LPCVD nitride.

(1) The $\pm$27V DC memory window size is similar for each cycling condition less than 10^{10} regardless of H_2 annealing for a field stress condition of E_n = 6 MV/cm and t_w = lusec, shown in Figure 4-26. For stress cycles greater than 10^{10}, the memory window of the non-anneled devices become larger. A memory window size of about 6.0 volts was maintained at each cycling condition. A 6.0 volt memory window was sustained up to 10^{10} cycles for the non-annealed case and increased to about 8.5 volts at 10^{11} cycles.

The voltage decay rate as a result of a ±27V 100usec pulse applied to the dual dielectric structure that had an H_2 anneal, did not change appreciably as a function of the number of endurance cycles, with stress condition E_n = 6 MV/cm, t_w = 1usec for either the cleared or written state. However, the decay rates appeared relatively high from the cleared state ranging from about 0.85V/decade to about 0.95V/decade for structures that were not annealed. The devices did not show any decay from the written state. This is due to the position of the written memory transistor threshold with respect to the non-memory transistor threshold of the structure. Up until about 10^{10} cycles there was no decay from the written state, with an 0.35V/decade rate occurring at 10^{11} cycles. The DSP structure again acts as a camouflage to the decay rate from the written state until the 10^{10} cycle point. At this point, the center of the memory has moved far enough in the negative direction to disallow the written state to be pulsed past the threshold voltage value of the non-memory transistor. Thus, the decay rate from the written state becomes visible at 10^{11} cycles.

The variation in ±20V DC window size for E_n = 7 MV/cm and t_w= 1usec is less for the devices that were annealed in H_2 when compared to the non-annealed results for the structures that consisted of the 374A LPCVD film. The range in window size was from 4.5 to 5.5 volts for the H_2 annealed condition.

The non-annealed window increased from 3.8V at 10^6 cycles to 4.8V at 10^7 cycles, becoming larger than the annealed devices between 10^6 and 10^7 level. At 10^8 cycles a window size of 6.4V was obtained and maintained through the 10^{10} point. The size decrease to 4.2V at 10^{11} cycles again become less than that of the annealed devices. The -29V clear and +27 write lusec pulse memory decay rates of memory gate structures consisting of a 374A LPCVD nitride after being stressed to 10^{11} cycles with a 6 MV/cm, lusec pulse were found to be 1.0V/decade for devices that were not annealed and 0.55/decode for those structures that were subjected to an H_2 anneal. The memory window size of the H_2 annealed subcells extrapolated to 0.3V after 24 hrs. subsequent to the 10^{11} cycle stress. The non-annealed structures experienced a complete collapse after about 2.2 hours. The pulse memory size of the non-annealed device was larger than the H_2 annealed device by about 25%, however, the voltage decay rate was larger by about 45%. The pulse memory window size and voltage decay rates for the stress conditions, E_n= 7 MV/cm and t_w= lusec, increased as the number of endurance cycles increased for both the annealed and non-annealed cases up until 10^9 to 10^{10} cycles. After 10^{10} cycles the memory window starts to decrease, however, the decay rate continues to increase. They decay rates were consistently lower for the H_2 annealed structures, and increased with endurance cycles at a slower rate than the non-annealed, however, the non-annealed film appears to be approaching a maximum, as has been observed and

reported in the literature. The decay rates range from 0.2V/decade after 10^5 cycles to 0.6V/decade after 10^{11} cycles for the H_2 annealed case, and from 0.33V/decade after 10^5 and 10^{11} endurance cycles respectively for the non-annealed condition. A data retention time of 24 hours was not obtained until the devices had been cycled to the 10^7 and 10^8 range. After 10^8 cycles memory window sizes of 0.5V for the annealed and about 1.0 for the non-annealed devices were maintained after 24 hours. The maximum window size was obtained at about the 10^9 to 10^{10} cycle range for each condition. A value of about 4.5V and 3.5V were determined for the non-annealed and H_2 annealed structures respectively. The memory window sizes after 24 hours at the 10^9 cycle point were 1.0 for the non-annealed case and 1.5 for the annealed condition. The extrapolated memory window size of an annealed device at 24 hours after 10^{11} endurance cycles was 0.5V. The non-annealed film had completely collapsed after 100 seconds. From these results it is surmised that a sufficient memory window is maintained after 10^{11} endurance cycles for the structures annealed in H_2 while the non-annealed devices have completely lost the window between 10^{10} and 10^{11} cycles. For the 7 MV/cm 1usec stress condition, the devices needed to be stressed above 10^7 endurance cycle to produce a memory window size large enough to maintain data for 24 hours.

A number of device types and structures have been evaluated with respect to total dose γ radiation suseptabilty. A dual

dielectric structure consisting of an oxide (77A) nitride (1457A) layer was used as the gate structure of the p-channel transistors fabricated in SOS. A 100% H_2 anneal was incorporated into the existing MNOS/SOS process sequence. It has been demonstrated that a post deposition H_2 anneal immediately following the memory nitride improves the endurance. Thus, it is important to determine to what extent annealing the fixed threshold devices in H_2 affects the radiation hardness. These structures were metal gate transistors ranging from 4um to 9um in length. The hardness was tested by subjecting the gate, drain and source-substrate to various bias conditions while the level of radiation was increased to 1M rad (Si). The gate bias of these structures was always negative or zero. A maximum voltage of -30V was applied either between the gate and source or the drain and source. Less than a two volt shift was observed up to about 100K rad (Si). This hardness level was noted for devices that had received the H_2 anneal and the one that did not.

The all oxide polysilicon gate capacitors that were fabricated in bulk silicon appear to have relatively good radiation characteristics even though this structure did have a silicon nitride deposited following polysilicon deposition, there was no subsequent H_2 anneal. The oxide was grown with a process sequence that included a dry cycle, a wet cycle followed by a short N_2 anneal. A temperature of 900^{o}C was used. A threshold voltage shift of less than 2V was observed

for a gate bias of 0V up to a total dose of 500K rads. Structues biased with +12V showed the same shift up to about 200K rads. It should be noted that those device that were biased with -8V and -18V shifted less than 2V after the 1M rad level.

The tolerance of the all oxide polysilicon gate transistor structures to total dose radiation was found to be quite low. The devices were fabricated using a MNOS/CMOS process that presently exist. The sequence includes a high temperature (1050°C) reflow anneal. The structure were also annealed in 100% H_2 at 900°C. Two oxide types were evaluated. A Dry-Wet-N_2 (DWN) and a Wet-Dry-N_2 (WDN) cycle. Devices with both oxide types were found to go into depletion at relatively low dose levels for all bias levels. The structures grown with the DWN process were not as susceptable to radiation damage as was the WDN sequence. However, the two oxides behave similarly in a γ radiation enviornment with a gate bias of 0V. A lateral shift was observed in the I_{DS} vs V_{GS} curves indicating an increase in charge associated with the gate dielectric. The slope change in the plots shows a degradation in the surface mobility as a function of total dose radiation. A number of variables could have been responsible for the observed degradation of these structures including the reflow anneal (1050°C) and/or the 100% H_2 anneal at 900°C. The fact that the capacitor structures showed relatively good radiation tolerance suggest promise in being able to produce an all oxide polysilion gate transistor that is radiation hard to an acceptable level.

6.0 CONCLUSIONS AND RECOMMENDATIONS

It was observed that the density of trapped charge increases as the NH_3:SiH_4 (APCVD), and NH_3:$SiCl_2H_2$ (LPCVD) ratio decreases. The SiH_4 films that were deposited with the low gas ratios (higher conductive layers) are expected to produce devices with faster pulse responses. This was observed to be case. However, the size of the memory window saturated at a relative low value. The films that were deposited with the higher gas ratios were found to have a larger saturated memory window. A dual deposition process where a "high" conductive film is deposited first and then a "low conductive film was found to perform with the speed of a single layer "high" conductive film. A saturated memory window size comparable to that of a single "low" conductive film was obtained. These results were consistent for structures processed with an APCVD first layer - LPCVD second layer and for a LPCVD first layer - LPCVD Second Layer.

When a thin silicon nitride film, 25A to 50A is annealed at elevated temperatures, 900 to 1100^{o}C the charge tunnel barrier is affected. The changes are manifested in the charge retention and pulse response. These parameters are further a function of the gas ambient, i.e. certain gases (e.g. NH_3) appeared to greatly reduce the charge decay rate and interface

state density, while other gases (e.g. H_2) reduced the amount of fixed positive charge in the bulk Si_3N_4 film. The structures that were annealed in N_2 were observed to have a larger pulse response.

Large amount of positive change were found to be present in the Si_3N_4 films of devices that were fabricated with the MNOS/SOS radiation hard process that did not receive any post Si_3N_4 anneals. However, the amount of fixed positive change was greatly decreased when a post deposition anneal in H_2 was performed. This conclusion was based on the fact that a positive shift between 1.5V and 2.5V in the non-memory transistor structure and the center of the memory window of the memory subcell structures occurred. The same effects were observed for capacitor structures. A positive shift of the memory window of capacitor structures was not accompanied by a decrease in interface state density charge. This substantiates that the positive charge in the bulk Si_3N_4 film is being reduced by the H_2 treatment.

All device structures that were post H_2 annealed experienced the 1.5V to 2.5V threshold voltage shift in a positive direction. The device structures with the all APCVD films and the ones deposited using the dual dielectric process with an APCVD nitride as a first layer and a LPCVD film as the second layer experienced a degradation in the film when annealed in H_2. The gates of a large percentage of the

devices were shorted or started to conduct relatively large amounts of current at low voltages (1 to 5 volts). This problem did not appear in the devices where the nitrides were an all LPCVD structure. This trend suggests that the H_2 anneals are deleterious to the integrity of the APCVD Si_3N_4 films. For this reason, continued investigation of the two step APCVD-LPCVD and single layer APCVD structure was discontinued for memory applications.

The following observations were made for MNOS/SOS memory cells that were fabricated without incorporating any anneals and for the condition where the structures were annealed in H_2 after the memory nitride was deposited:

(1) The voltage decay rate increased monotonically with endurance cycles, however the rate for the unannealed structure was larger than for the H_2 annealed device (stress conditions of 6MV/cm and 7Mv/cm and 1usec pulse width.)

(2) Each type structure requires that the devices be cycled a prescribed number of times before a memory window size is obtained which is large enough to maintain a 1.0 volt level after 24 hours, after being pulsed with a 1usec, 7MV/cm initial nitride field.

(3) A 1.0 volt memory window was maintained for H_2

annnealed structures after 10^{11} cycles at a field level of 7 Mv/cm with a pulse width of 1u sec. The devices that were not annealed collapsed after less than an hour after being stressed with the same conditions.

Transistor structures that were subjected to an accelerated stress condition experienced an increase in the interface state density. A positive V_{GS} of 27V (E_{no}=7.0 MV/cm) was produced by forcing a current density of I = 10^{-6} A (J = 7.2mA/cm^2) through the Si_3N_4 film.

The results of capacitor structures with X_n ranging from 400A to 1000A indicated that the time to breakdown was not a function of nitride thickness. The stress condition for these structures were I = 10^{-6} A (J= 3.2 mA/cm_2) and E_{no} = 7.0 mV/cm. It was observed that the average time to breakdown for structures that was annealed and oxidized prior to metalization increased by at least an order of magnitude.

From the above conclusions it is observed that annealing in H_2 improves the endurance and retention properties of the MNOS memory structure. With this it is recommended that in order to achieve reliable operations of MNOS memory devices to at least 10^{11} clear/write cycles, for a pulse duration of 1u sec with a nitride field between 6MV/cm and 7MV/cm that a post memory nitride deposition anneal be introduced into the process.

The N-channel all oxide polysilicon gate transistors fabricated with an existing MNOS/CMOS process were not found to be suceptable to total dose radiation. Capacitor structures that were fabricated using sements of the above process showed relatively good radiation tolerance. Even though these structures did not receive the H_2 anneal, it is felt that the radiation susceptability will not be degraded very much if any when subjected to a high temperature anneal. It cannot be determined, with the data that is presently available, to what extent, if any, either of the high temperature steps degraded the radiation hardness of these structures. Preliminary data on capacitor structures, however, shows promise in obtaining an all oxide polysilicon gate transistor that is radiation hard to acceptable levels.

7.0 REFERENCES

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